



H11H4-AD2

V:1.1

ECS
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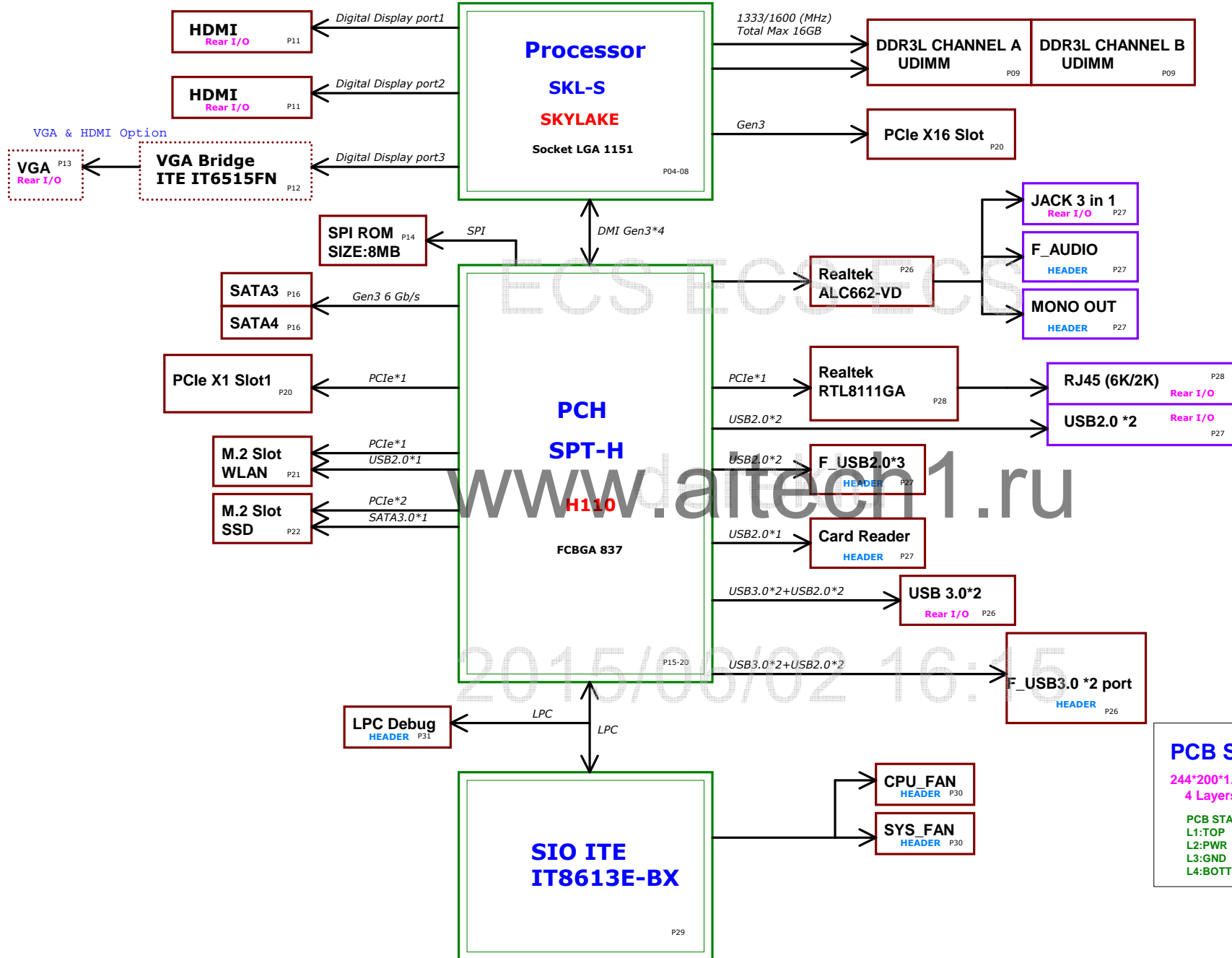
HSIO Lane Assignments by SKU (Lanes 1-14)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
USB3 #1 (Dual Mode)	USB3 #2	USB3 #3	USB3 #4	USB3 #5	USB3 #6	USB3 #7	USB3 #8	USB3 #9	USB3 #10	USB3 #11	PCIe #5	PCIe #6	PCIe #7	PCIe #8
	SSIC #1	SSIC #2					PCIe #1	PCIe #2	PCIe #3	PCIe #4	CbE	CbE		
								X4				X4		
								X2	X2			X2	X2	
														N/A
sku	1	2	3	4	5	6	7	8	9	10	11	12	13	14
H110	USB3/OTG	USB3/SSIC	USB3/SSIC	USB3	N/A	N/A	N/A	N/A	N/A	LAN Only	PCIe/LAN	PCIe	PCIe	PCIe
B150	USB3/OTG	USB3/SSIC	USB3/SSIC	USB3	USB3	USB3	N/A	N/A	N/A	LAN Only	PCIe/LAN	PCIe	PCIe	PCIe
Q150	USB3/OTG	USB3/SSIC	USB3/SSIC	USB3	USB3	USB3	USB3	USB3	N/A	LAN Only	PCIe/LAN	PCIe	PCIe	PCIe
H170	USB3/OTG	USB3/SSIC	USB3/SSIC	USB3	USB3	USB3	USB3	USB3	PCIe	PCIe/LAN	PCIe/LAN	PCIe	PCIe	PCIe
Z170	USB3/OTG	USB3/SSIC	USB3/SSIC	USB3	USB3	USB3	PCIe	PCIe	PCIe	USB3/PCIe/LAN	PCIe/LAN	PCIe	PCIe	PCIe
E170	USB3/OTG	USB3/SSIC	USB3/SSIC	USB3	USB3	USB3	PCIe	PCIe	PCIe	USB3/PCIe/LAN	PCIe/LAN	PCIe	PCIe	PCIe

HSIO Lane Assignments by SKU (Lanes 15-26)

	15	16	17	18	19	20	21	22	23	24	25	26
	PCIe #9	PCIe #10	PCIe #11	PCIe #12	PCIe #13	PCIe #14	PCIe #15	PCIe #16	PCIe #17	PCIe #18	PCIe #19	PCIe #20
	SATA #0	SATA #1			SATA #0**	SATA #1**	SATA #2	SATA #3	SATA #4	SATA #5		
	CbE			CbE	CbE							
			X4			X4		X4		X4		
			X2	X2		X2	X2		X2	X2		
												Intel® RST for PCIe Storage
sku	15	16	17	18	19	20	21	22	23	24	25	26
H110	PCIe/LAN	PCIe	N/A	LAN Only	SATA*/SATA*	SATA*	SATA	SATA	N/A	N/A	N/A	N/A
B150	PCIe/LAN	PCIe/SATA*		PCIe/LAN	SATA*/SATA*	SATA*	SATA	SATA	SATA	SATA	N/A	N/A
Q150	PCIe/LAN	PCIe/SATA	PCIe	PCIe/LAN	PCIe/LAN	PCIe/LAN	SATA	SATA	SATA	SATA	N/A	N/A
H170	PCIe/LAN	PCIe/SATA	PCIe	PCIe/LAN	PCIe/LAN	PCIe/LAN	PCIe/SATA	PCIe/SATA	SATA	SATA	PCIe	PCIe
Z170	PCIe/LAN	PCIe/SATA	PCIe	PCIe/LAN	PCIe/LAN	PCIe/LAN	PCIe/SATA	PCIe/SATA	SATA	SATA	PCIe	PCIe
E170	PCIe/LAN	PCIe/SATA	PCIe	PCIe/LAN	PCIe/LAN	PCIe/LAN	PCIe/SATA	PCIe/SATA	SATA	SATA	PCIe	PCIe

Skylake-S Desktop Platform



PCB SIZE

244*200*1.6mm
4 Layers

PCB STACK:
L1:TOP
L2:PWR
L3:GND
L4:BOTTOM

PCH-GPIO function		Data:2014/11/28	
Pin Name	Power Well	Usage	Boot Set
GPP_F17	3VSB	LPC_PME_L	PME#
GPD10	ATX_3VSB	GPD10_DIS_ME	GPO
GPP_B13	N/A	PCH_PLTRST_L	PLTRST#
GPP_G16	3VSB	IOAC	GPO
GPP_G13	VCC3	HDPANEL_DETECT	GPI
GPP_E7	VCC3	THERMAL_SD	GPI
GPP_B3	3VSB	BT_DIS_L_R	GPO
GPP_H18	3VSB	GPP_H18	GPI
GPP_H17	3VSB	GPP_H17	GPI
GPP_H16	3VSB	GPP_H16	GPI
GPP_H15	3VSB	GPP_H15	For Acer Reserve
GPP_H14	3VSB	GPP_H14	For Acer Reserve
GPP_B14	+VCC3	PCH_SPKR	SPKR
GPP_A14	3VSB	LPCPD_L	SUS_STAT#
GPP_C6	3VSB	SML1_CLK	SML1CLK
GPP_C7	3VSB	SML1_DATA	SML1DATA
GPP_E8	VCC3	SATALED_L	SATALED#
GPP_E0	VCC3	SSD_DETECT_L	GPI
GPP_E4	VCC3	DEVSLP0	SATA_DEVSLP0
GPP_F22	VCC3	PCIE16RST	GPO
GPP_F14	3VSB	H_SKT0CC_L	GPI
GPP_B17	3VSB	M2_DIS_L_R	GPO
GPP_B6	VCC3	CLK_REQ1_M2_WLAN_L	SRCLKREQ1#
GPP_B8	VCC3	CLKREQ3_SSD_L	SRCLKREQ3#

SIO-GPIO function		Data:2014/11/28	
Pin Name	Power Well	Usage	Default SET
PCH_D0B/GP22	+ATX3VSB	Front Panel LED contral (SIO_LED1)	GPO
GP21	+ATX3VSB	Front Panel LED contral (SIO_LED0)	GPO
PCIRST1#(PCH_COA/GP12	3VSB	SML1_CLK	PCH_COA
VCORE_EN/GP42/	3VSB	SUSWARN_R	SUSWARN
PCH_C0B/SUSWARN#			
DSR1#/GP45/PCH_D0A	3VSB	SML1_DATA	PCH_D0A
CTS1#/GP31/FAN_TAC5	VCC3	THERMAL_SD	
VLDT_EN/SLP_SUS#/GP63	+ATX3VSB	SLPSUS_L	SLP_SUS#
SUSACK#/PWRGD1	3VSB	SUSACK_R	SUSACK#

Interrupt mapping		Data:2014/11/28	
Function	INT# port	PCle*1 port	Device
M. 2 (WLAN)	INTB#	Port 10	Wireless LAN
LAN	INTB#	Port 6	RTL8111GA
SATA	INTA#	NA	SATA3.0
M. 2 (SSD)	INTC#	Port 7	SSD
PCIeX1	INTA#	Port 5	PCIeX1

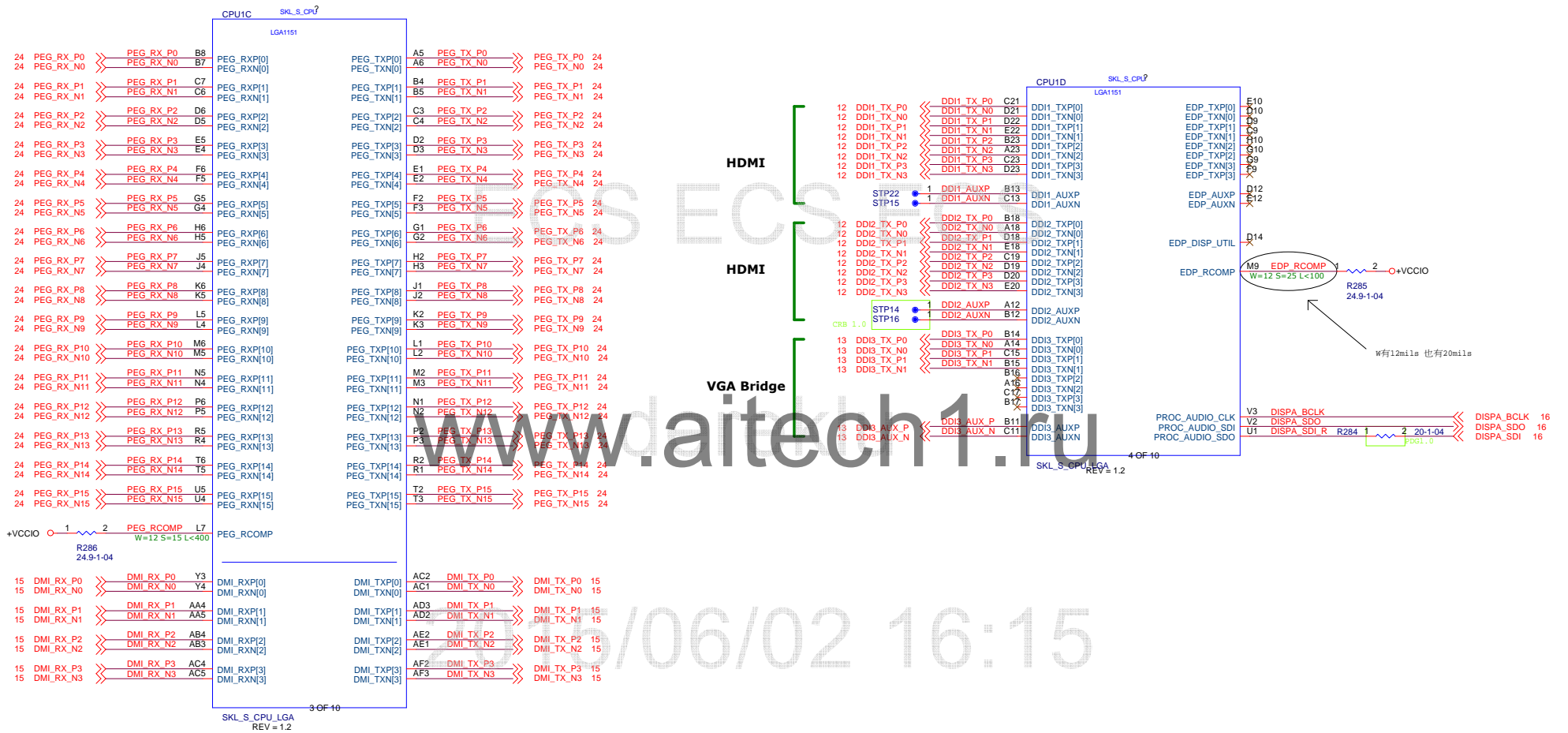
Strap Setting		Data:2014/11/28	
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Schematics Version History Table:			Data:2014/11/28	
Rev.	Date	Page	Change list	Remark
B	20150121	7,38	C312,C301,C313,C302 ->DelC39, 33U-10VX7-06 -> 22U-25VX7-06 R122 27.4K-1-04 -> 47.5K-1-04;R117 3.74K-1-04 ->4.99K-1-04 R111 56K-04 ->88.7K-1-04;C72 1200P-50VX7-04 -> 3300P-50VX7-04 C644 220P-50VX7-04 -> 330P-50VX7-04;R67 1K-1-04 -> 510-1-04	Vcore power solution.
	20150121	38,40	R165 11K-1-04 -> 15K-1-04; R175 7.5K-04 -> 36K-04 C175 1200P-50VX7-04 -> 560P-50VX7-04; R204 3.6K-04 -> 1K-04 C187 680P-50VX7-04->1800P-50VX7-04; R194 1K-04 -> 200-04 Del: SC35	VGT power solution.
	20150121	38,40	R196 3.3K-1-04 -> 4.99K-1-04; Del:SC22	VSA power solution.
	20150121	38	R165 11K-1-04 -> 15K-1-04; R175 7.5K-04 -> 36K-04 C175 1200P-50VX7-04 -> 560P-50VX7-04; R204 3.6K-04 -> 1K-04 C187 680P-50VX7-04->1800P-50VX7-04; R194 1K-04 -> 200-04	VCC leakage issue in sleep S3.
	20150121	38,41	R143 22K-04 -> unstuff; R323 unstuff -> 20K-04	VR_Ready sequence issue in Power on.
	20150121	41	R704 10K-04->4.99K-1-04; R693 4.7K-04->20K-1-04 R666 8.2K-04 -> 8.2K-1-04; R667 750-1-04 ->2.4K-1-04	VCCIO POWER Sequence issue.
	20150121	42	L19 footprint CHOKE_1R5_SMD_2P change to CHOKE_PT5D45MM_SMD	NPI issue
	20150121	42	R398 unstuff->100K; R688 4.7K-> unstuff L22,L23 BOM change from INC0809-1ROM-JY1YW to INC0809-1ROM-JY1YW	VDIMM Power sequence issue Power issue
	20150121	32	Add circuit for DPWROK + +ATX_3VSB power down sequence timing issue.	
	20150121	32	Add circuit for RSMRST + +V1P0A power down sequence timing issue.	
	20150121	11	Add C428,C398,C436 (22U-6V3X5-08)	VRRF DC noise.
	20150121	12	Add C47,C46,C31,C12 unstuff -> 470P-50VX7-04 Add reserve C56,C77,C95,C87	Solve DDC signal test fail.
	20150121	13,14,27,29,30	C14 unstuff -> 1U-6V3X5-04; C4 unstuff -> 4.7U-6V3X5-06 C14 - SC9 - SC7 - C3 - C468 - C629 - C122 - C284 - C120 - C97 - C117 unstuff -> .1U; C8 - C7 unstuff -> 27P-04; C51 unstuff -> 1U-6V3X5-04 C139-C146 unstuff -> 2.7P-04 L8 - L7 unstuff ->CMK-90-08-MUT1-TAITECH; C105,C118,C119Unstuff -> 470P-50VX7-04	EMI solution.
	20150121	26	U33 - U15 change from UP7556 to UP7537	Safety solution
	20150121	33	Q38 Pin change from LAN_LED0 to LAN_LED2.	Solve Front LAN LED issue
	20150121	33	C554 - C599 unstuff -> .1U-16VX7-04	Acer PUS AVLC request.
	20150121	39	Minimun Load circuit modify	
	20150121	21	Remove WLAN LED BOM	
	20150121	17,18	SC43,SC42 Z2P->15P; Add SR36 0-04 C588,C592 18P->15P; R662 22-04 -> 33-1-04 R722 22-04 -> 47.5-1-04	CLK solution
	20150121	15	R610 unstuff -> 15K-04 R597 1.2K-1-04 -> unstuff	MDM-04 Update
	20150302	6	R273 22-04 -> 26-04	Follow PDG
	20150302	12,14	C77 - C86 - C87 - C85 unstuff -> 105P-04;C16 unstuff -> 1000P-50VX7-04	EMI solution
	20150302	14	C30 unstuff ->1U-25VX5-04; C8 - C7 unstuff -> 27P-04;R722 47.5-1-04 -> 56-1-04	SI solution.
	20150302	16,24	Add PCIeX16/X1 PRSNT# circuit	CLK Auto detect
	20150302	22	PCIe Port 7 - 8 Sawp for PCI Express Controller Lane Reversal	Follow PDG1.5 Update
	20150302	22	Remove LAN Power circuit.	By EuP test PASS
	20150302	37	Add C558,C645 10U	220W PSU noise solution
	20150310	7,38-42	Power cost down	
	20150302	43	R440 4.7K-04 -> unstuff for +3VSB leakage solution in EuP mode .	

Schematics Version History Table:			Data:2014/11/28	
Rev.	Date	Page	Change list	Remark
1.0	20150518	13,14	VGA change to Reserve	
	20150518	12	C31,C12,C46,C47 unstuff -> 470P-50VX7-04	HDMI DDC sloution for SI test.
	20150518	15	R610 1K-04->unstuff;R597 unstuff -> 1.21K-1-04	For PCH QS pull-down 1.21K
	20150518	17,32	R662 33-1-04 -> 56-1-04;C613 unstuff -> 10P-04	24M CLK solution for SI test.
	20150518	32	Reserve RSMRST& Power down sequence circuit.	For iPCH21 power sequence pass.
	20150518	21	R357 unstuff ->10K-04;R432 unstuff->0-04 R426 unstuff->0-04	Auto control CLK
	20150518	15	ME test - SPI_Debug - LPC_Debug header change to Reserve.	MP request
	20150518	37	C598 unstuff -> .1U-16VX7-04;C531 unstuff-> 22-16VX5-04	EMC solution
	20150518	39	C596 unstuff -> .1U16VX7-04	
	20150518	32	Z2,Z3 footprint change to short pad. R639 change from 4.7k to 510 for iPCH16 of B BOM issue.	

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GPIO Function/INT# Mapping			
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DDR3L CH.A

9	M_DATA_A[0..63]	<<<	M_DATA_A[0..63]
9	M_CLK_A_P[0..1]	<<<	M_CLK_A_P[0..1]
9	M_CLK_A_N[0..1]	<<<	M_CLK_A_N[0..1]
9	M_CKE_A[0..1]	<<<	M_CKE_A[0..1]
9	M_CS_A_L[0..1]	<<<	M_CS_A_L[0..1]
9	M_ODT_A[0..1]	<<<	M_ODT_A[0..1]
9	M_BS_A[0..2]	<<<	M_BS_A[0..2]
9	M_MA_A[0..15]	<<<	M_MA_A[0..15]
9	M_DQS_A_P[0..7]	<<<	M_DQS_A_P[0..7]
9	M_DQS_A_N[0..7]	<<<	M_DQS_A_N[0..7]
9	M_RAS_A_L	<<<	M_RAS_A_L
9	M_WE_A_L	<<<	M_WE_A_L
9	M_CAS_A_L	<<<	M_CAS_A_L

DDR3L CH.B

9	M_DATA_B[0..63]	<<<	M_DATA_B[0..63]
9	M_CLK_B_P[0..1]	<<<	M_CLK_B_P[0..1]
9	M_CLK_B_N[0..1]	<<<	M_CLK_B_N[0..1]
9	M_CKE_B[0..1]	<<<	M_CKE_B[0..1]
9	M_CS_B_L[0..1]	<<<	M_CS_B_L[0..1]
9	M_ODT_B[0..1]	<<<	M_ODT_B[0..1]
9	M_BS_B[0..2]	<<<	M_BS_B[0..2]
9	M_MA_B[0..15]	<<<	M_MA_B[0..15]
9	M_DQS_B_P[0..7]	<<<	M_DQS_B_P[0..7]
9	M_DQS_B_N[0..7]	<<<	M_DQS_B_N[0..7]
9	M_RAS_B_L	<<<	M_RAS_B_L
9	M_WE_B_L	<<<	M_WE_B_L
9	M_CAS_B_L	<<<	M_CAS_B_L

Follow DDR4 RVP8 CRB

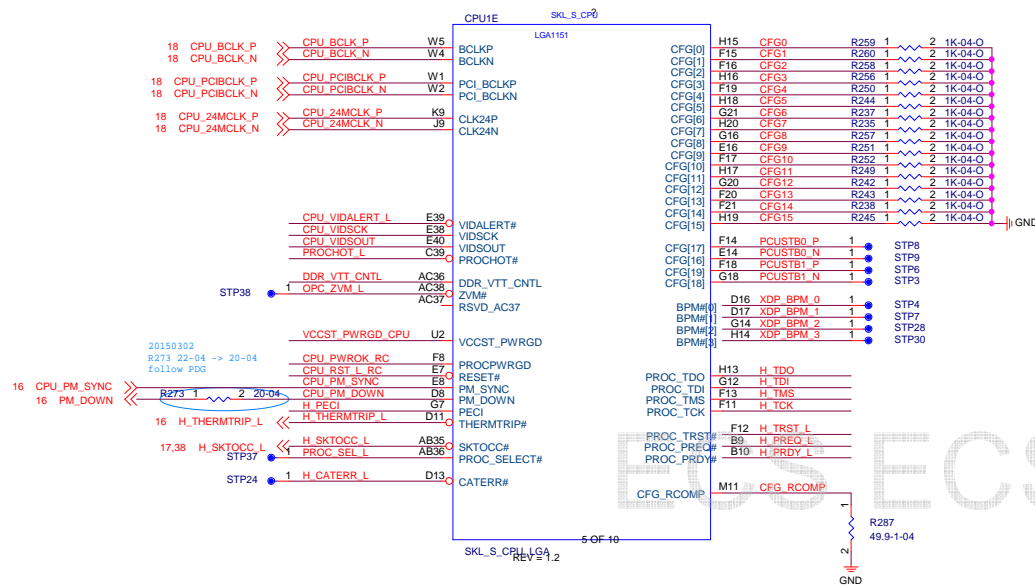
****Attention**



Follow DDR4 RVP8 CRB

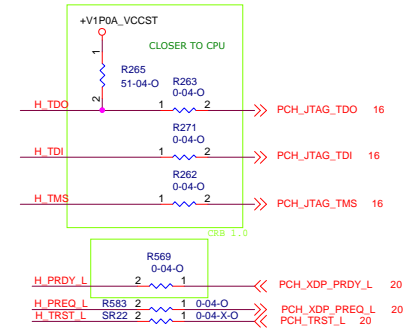
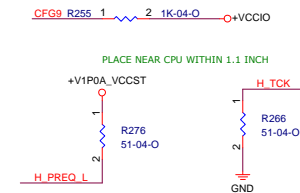
****Attention**



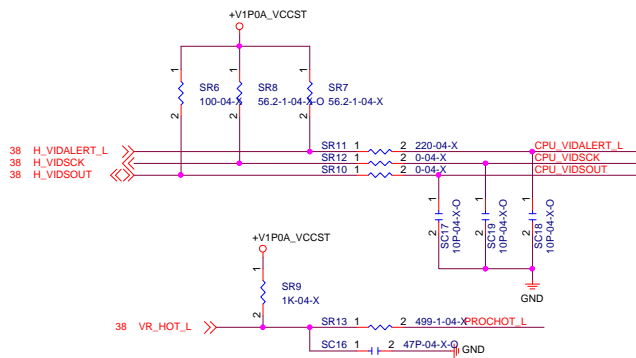


CFG[0:15] Configuration note

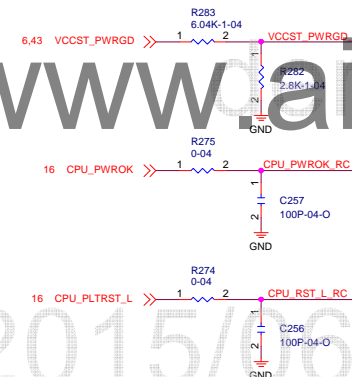
- CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted:
 - 1 = (Default) Normal Operation; No stall.
 - 0 = Stall.
- CFG[1]:** Reserved configuration lane.
- CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal.
 - 1 = Normal operation
 - 0 = Lane numbers reversed.
- CFG[3]:** Reserved configuration lane.
- CFG[4]:** eDP enable:
 - 1 = Disabled.
 - 0 = Enabled.
- CFG[5]:** PCI Express* Bifurcation
 - 00 = 1 x8, 2 x4 PCI Express*
 - 01 = reserved
 - 10 = 2 x8 PCI Express*
 - 11 = 1 x16 PCI Express*
- CFG[7]:** PEG Training:
 - 1 = (default) PEG Train immediately following RESET# de-assertion.
 - 0 = PEG Wait for BIOS for training.
- CFG[19:8]:** Reserved configuration lanes.



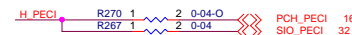
Asynchronous & Sideband Signal



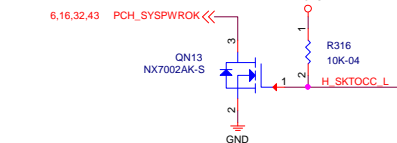
Processor Power Good



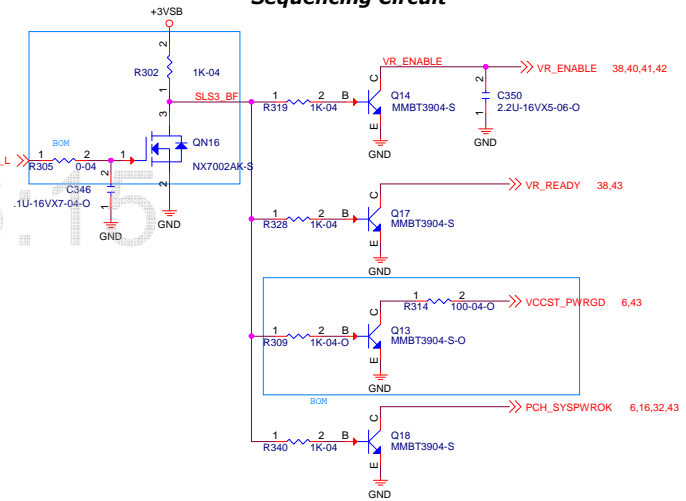
PECI



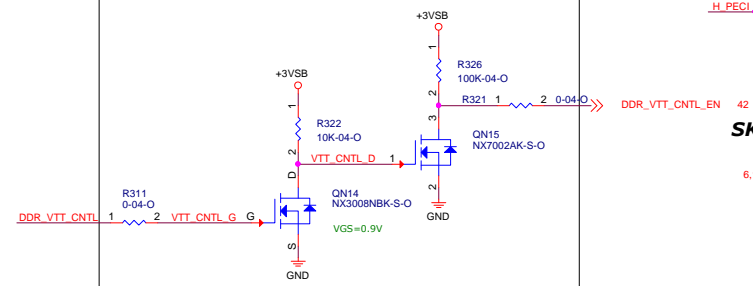
SKTOCC#



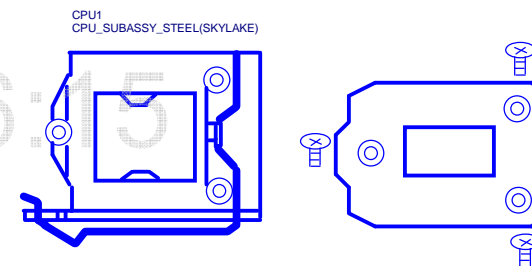
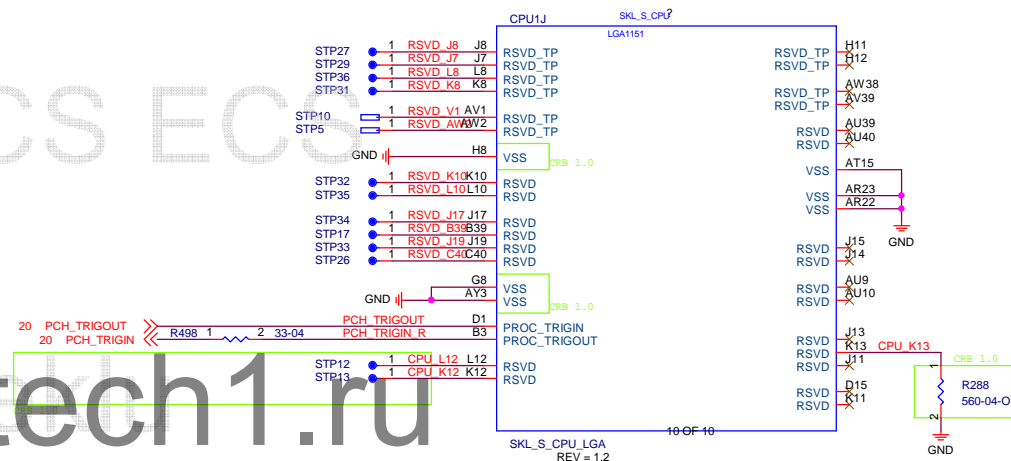
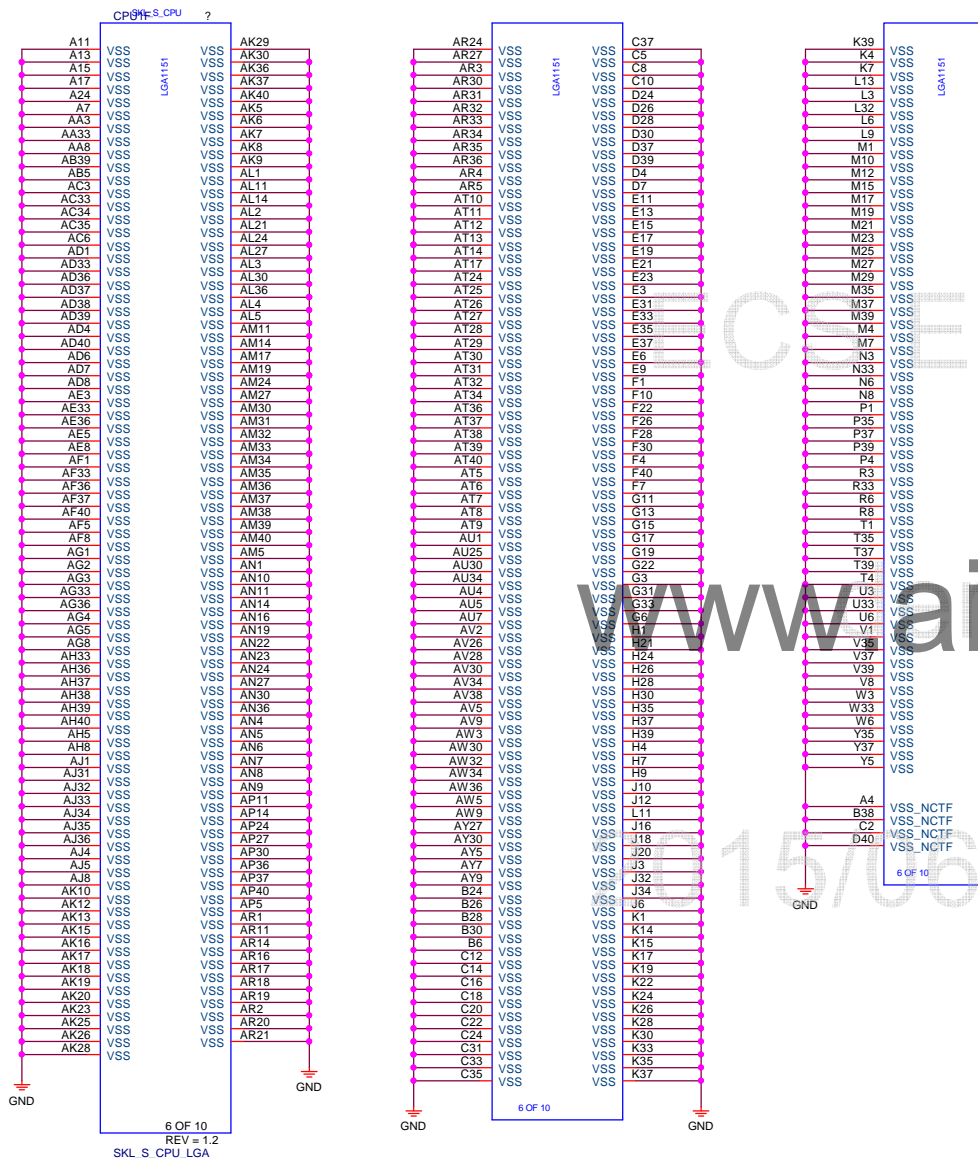
Sequencing Circuit



DDR_VTT Disable



Elitegroup Computer Systems			
Title	CPU-MISC		
Size	Document Number	H11H4-AD2	Rev V1.1
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CPU Steel (T/U pahse)
 PN:20-800-005911 SUBASSY.STEEL....LGA 1155/1156P.W/BACK PLATE.....
 ACA-ZIF-082-P38....LEAD-FREE(RoHS/HF).LOTES

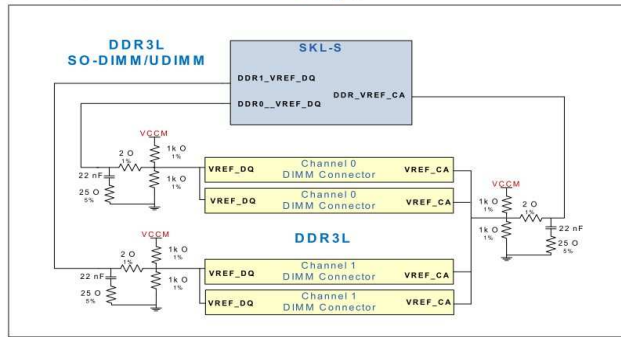
CPU Socket (SMD phase)
 PN:11-018-115133 SOCKET.CPU..LGA 1151P SMD..G/F...
 BLACK.AZIF0049-P002C...HF.LEAD-FREE.LOTES

ECS ECS ECS

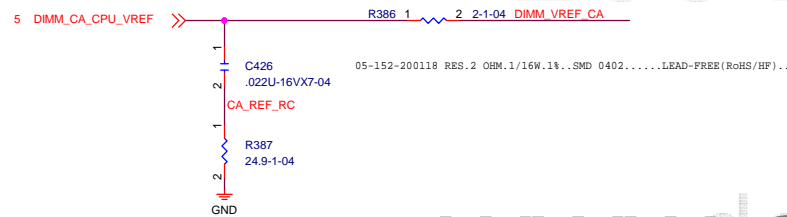
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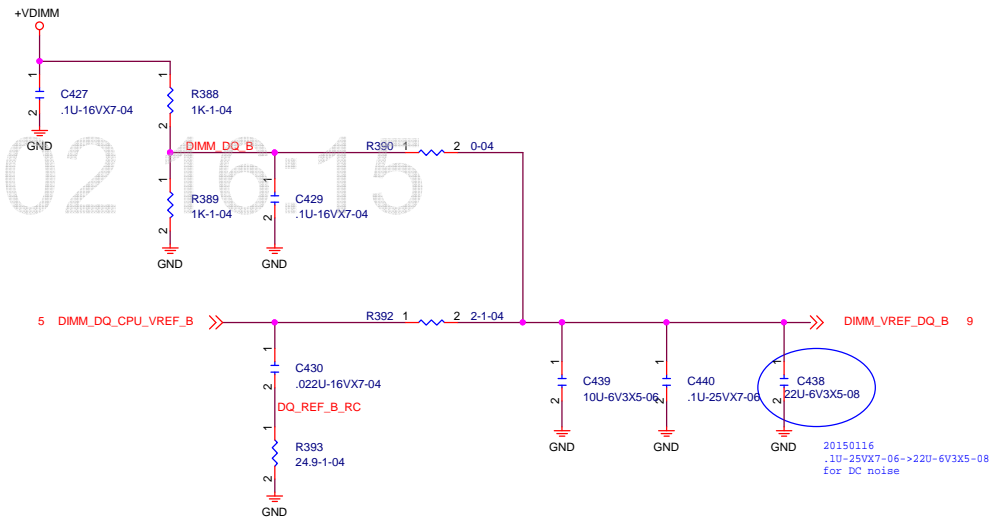
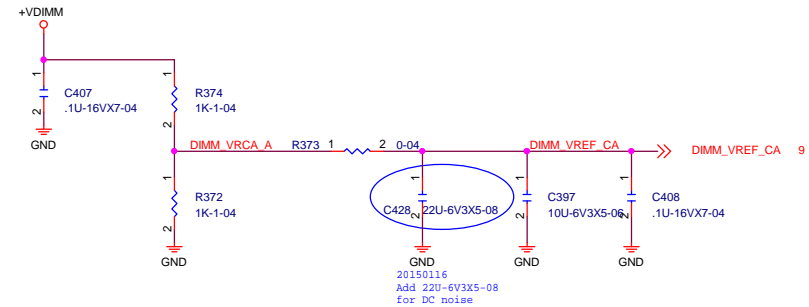
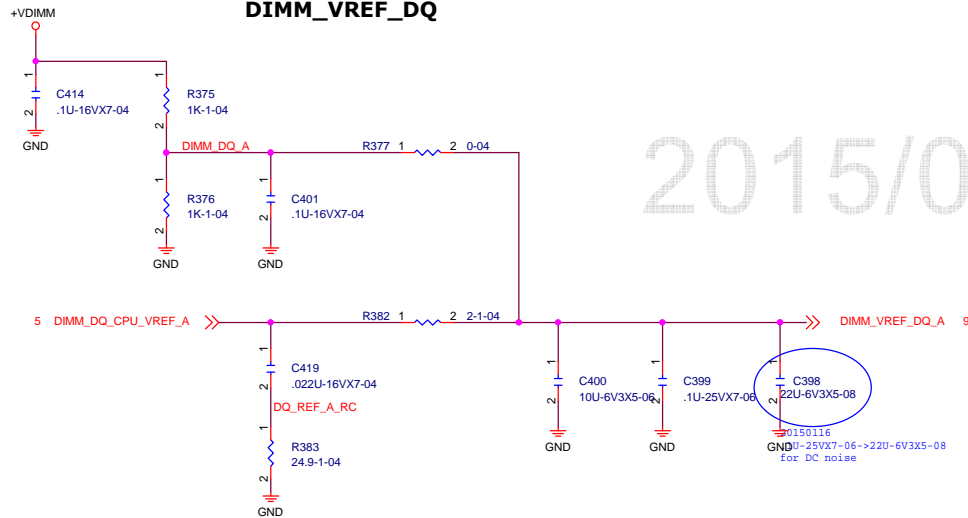
Figure 4-12. DDR3L SODIMM and UDIMM VREF Topologies

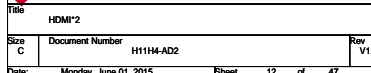


DIMM_VREF_CA

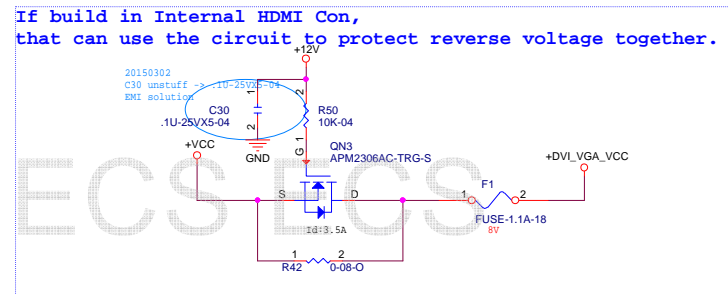
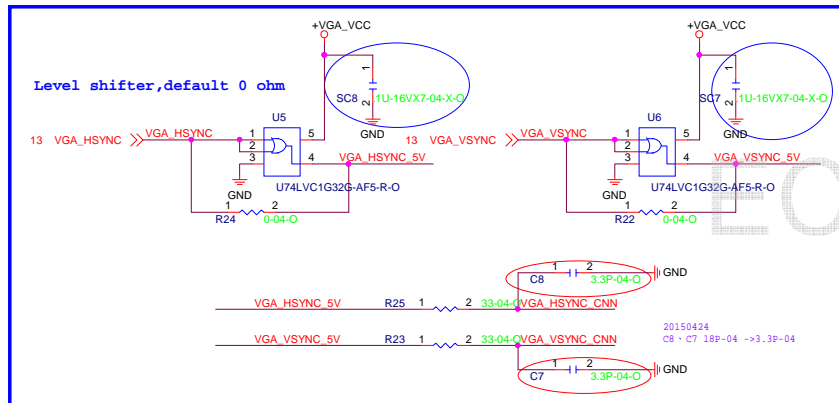
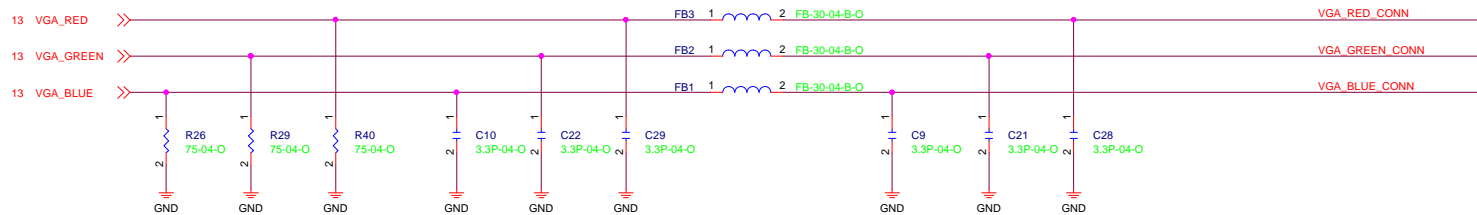


DIMM_VREF_DQ

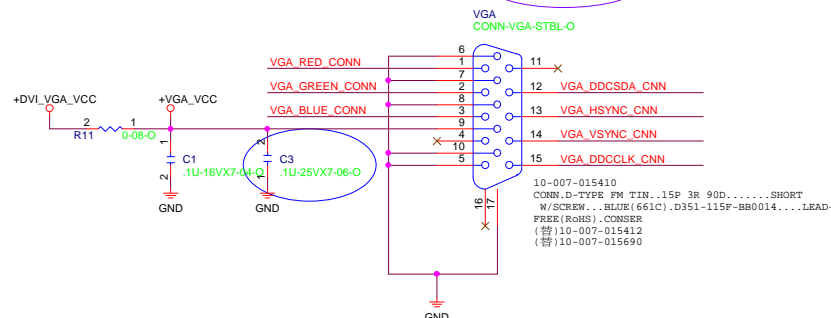
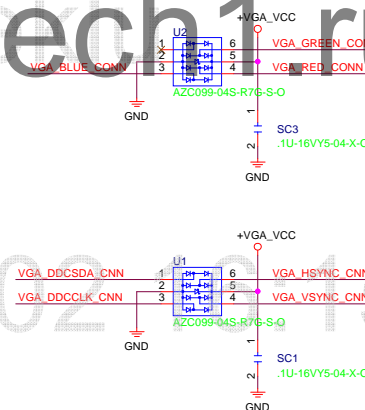
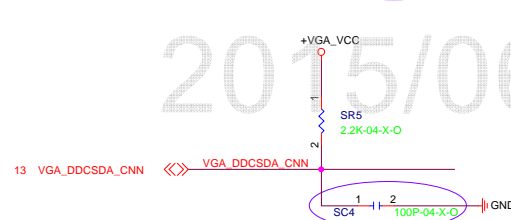
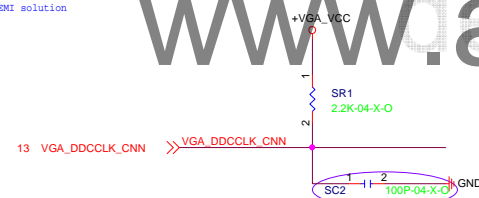




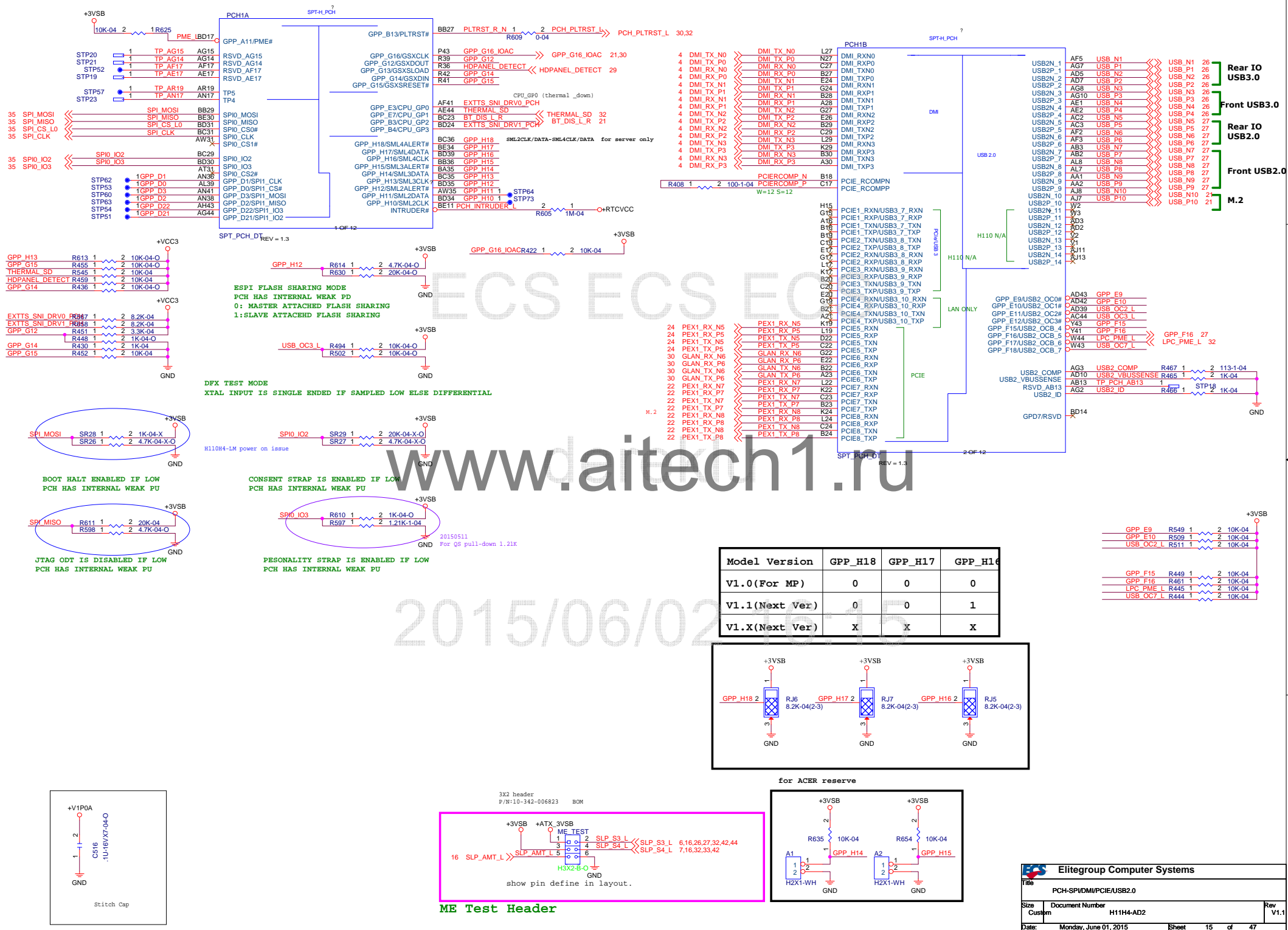
VGA (VGA & DP Option)

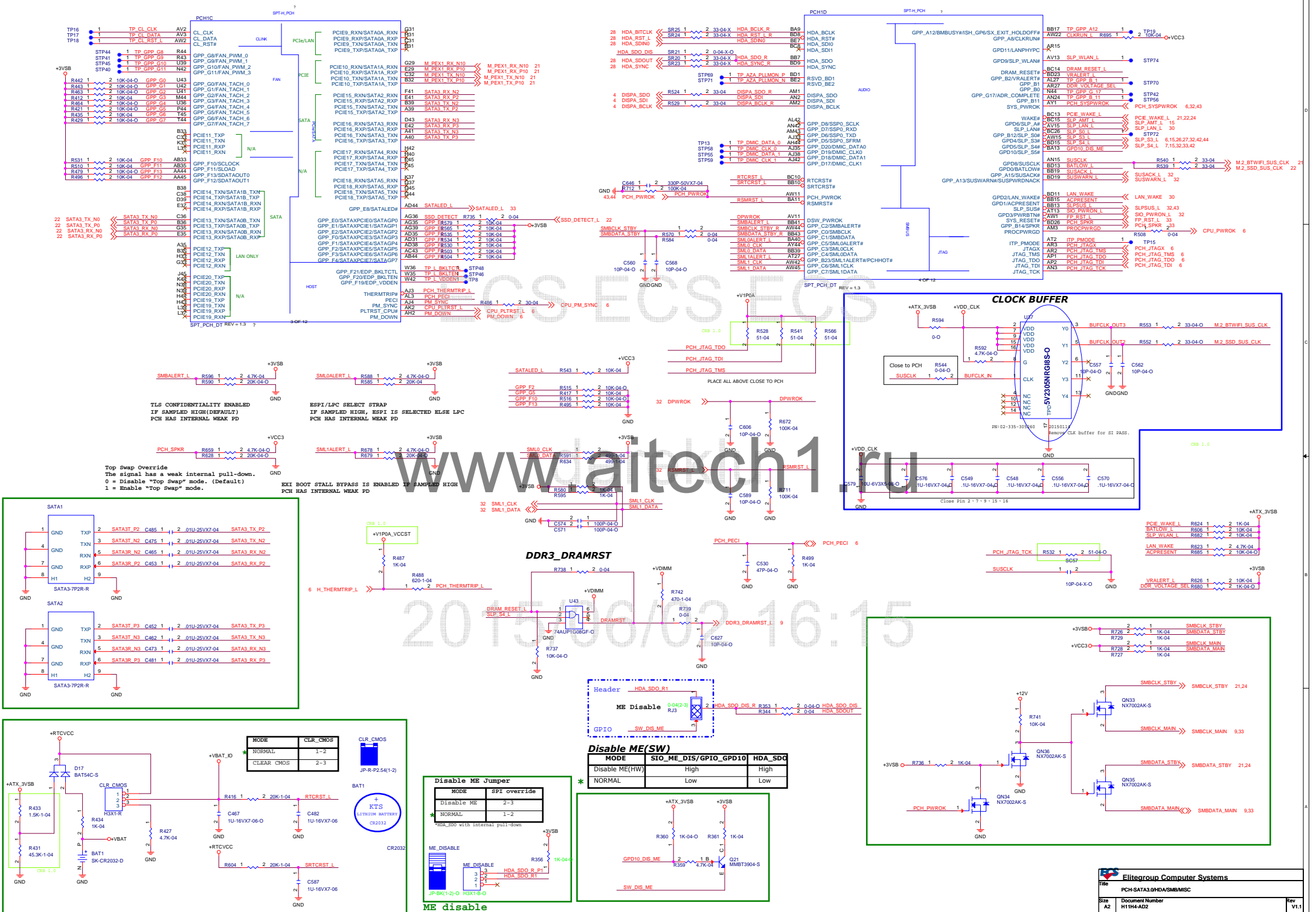


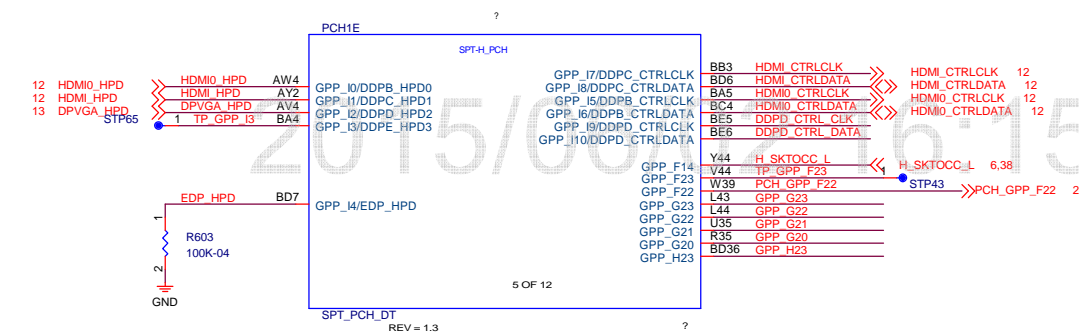
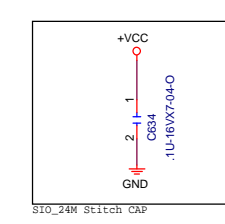
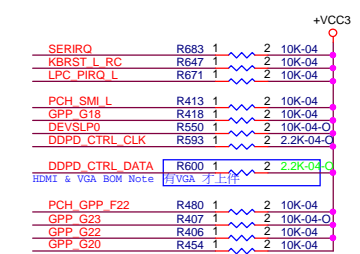
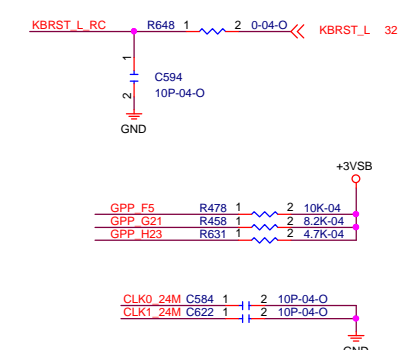
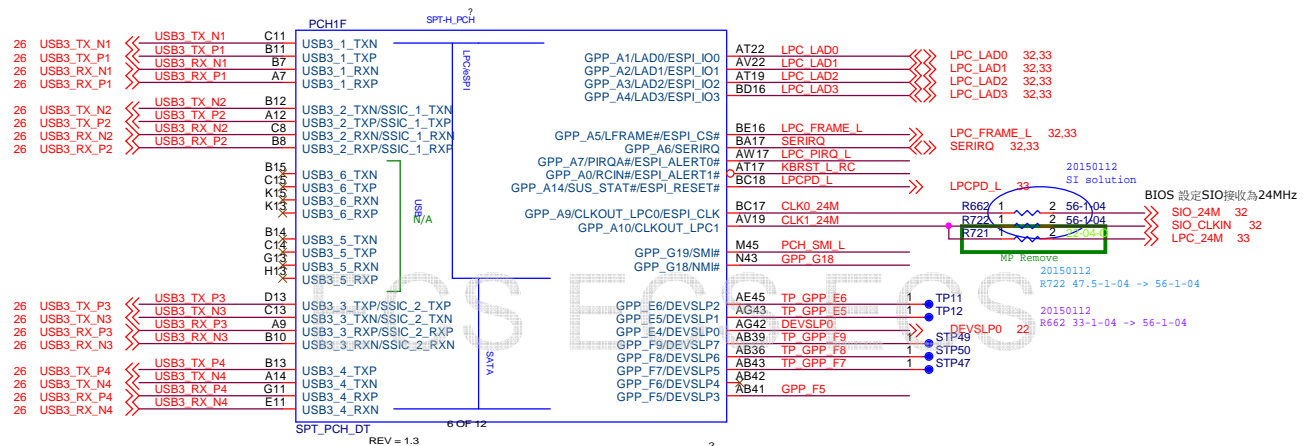
20150112 SC8 - SC7 - C3 unstuff -> -1P RMI solution



Elitegroup Computer Systems			
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Size Custom	Document Number H11H4-AD2	Rev V1.1	
Date Monday, June 01, 2015	Sheet 14	of 47	

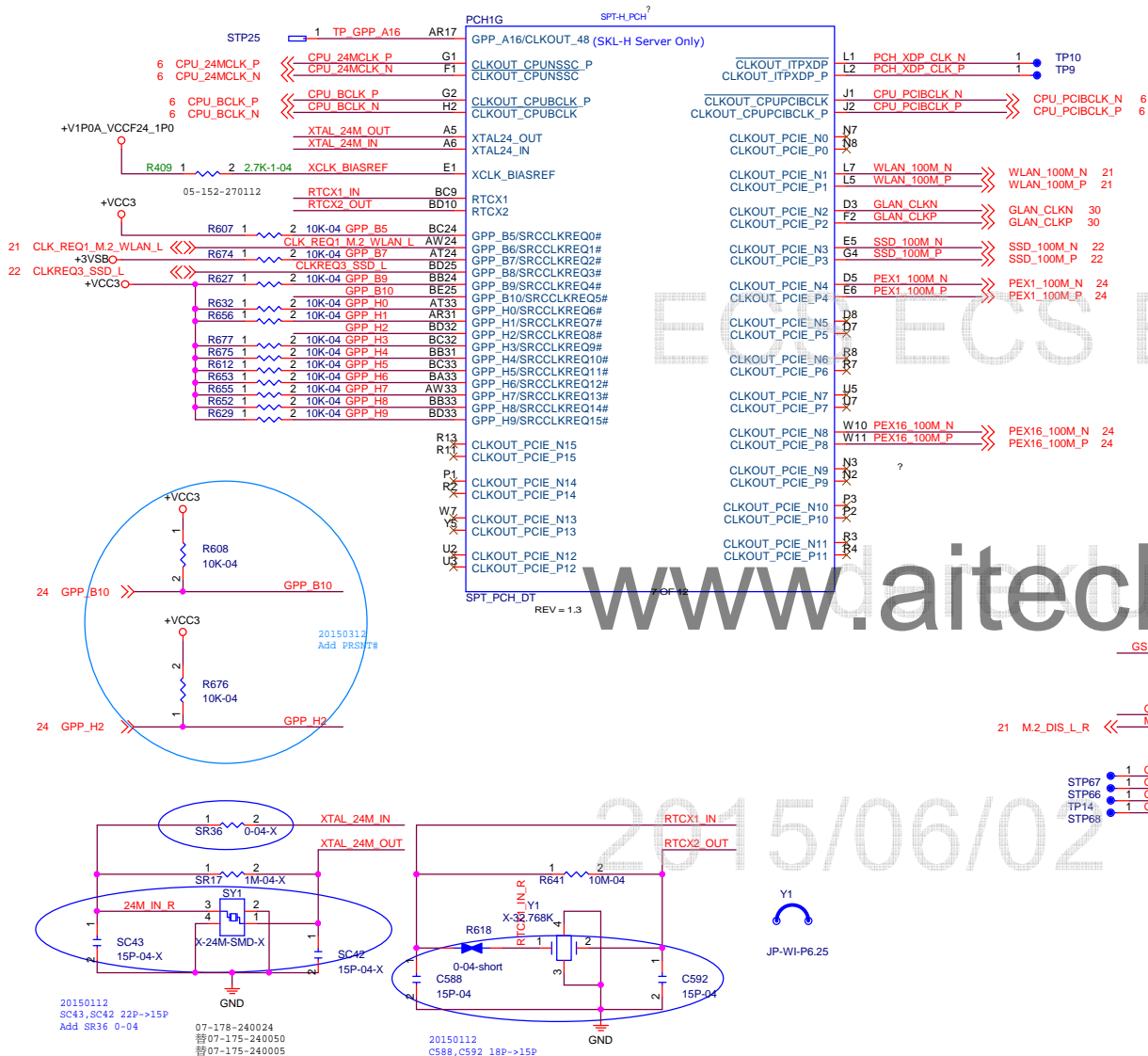






follow PDG eDP Disabling need Pull down to ground via 100k ohm resistor

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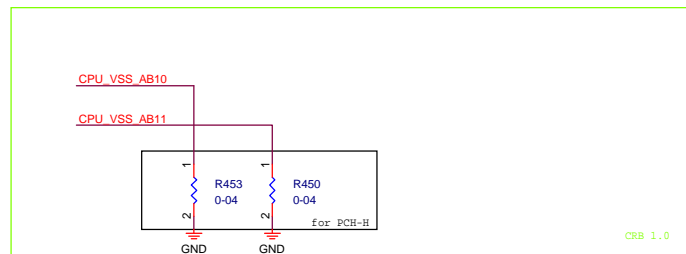
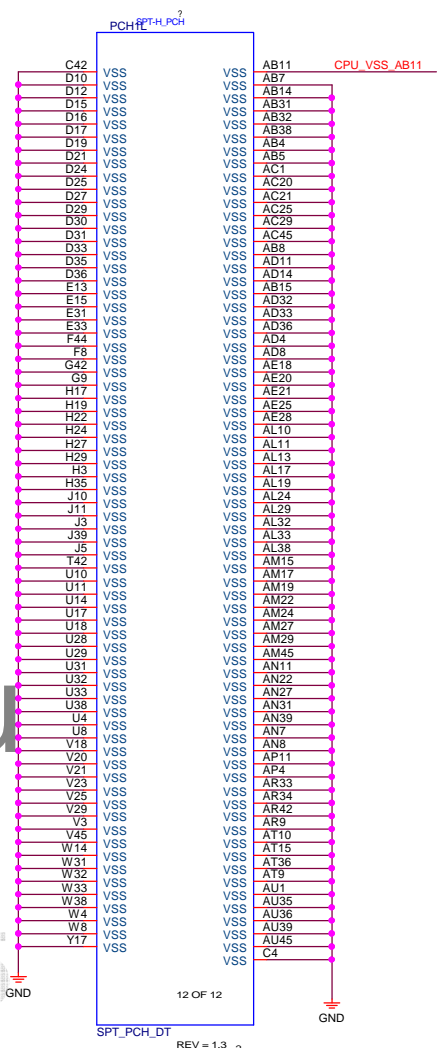
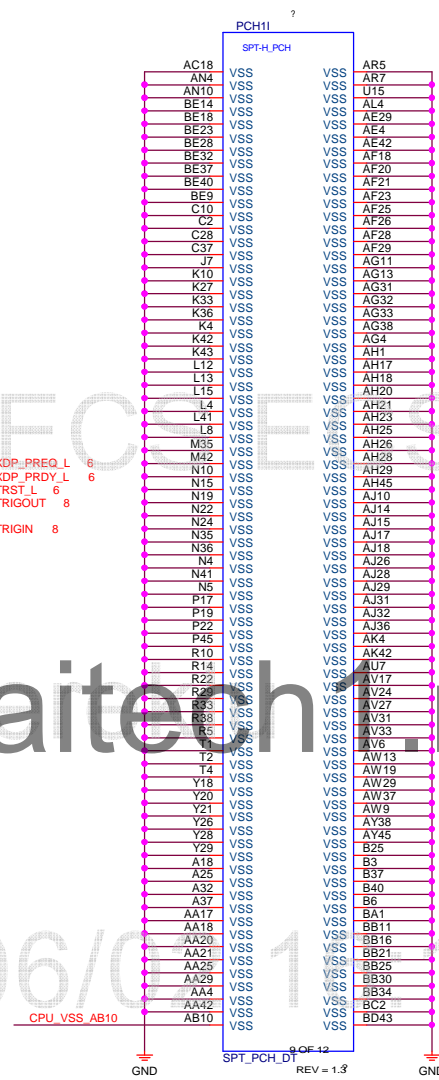
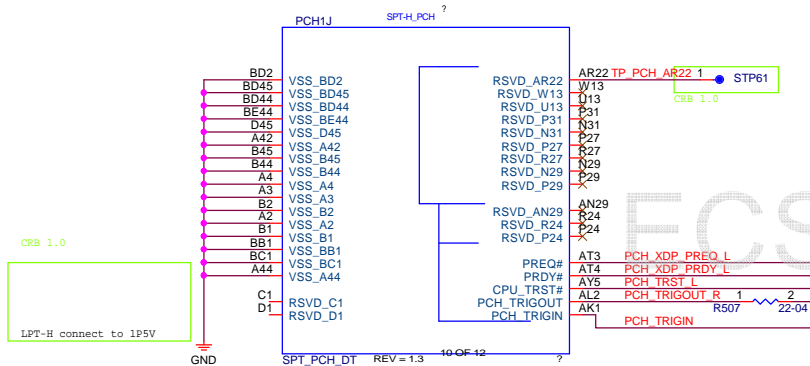
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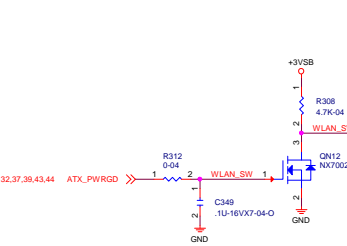
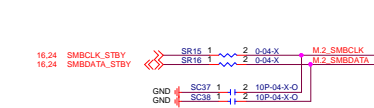
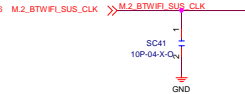
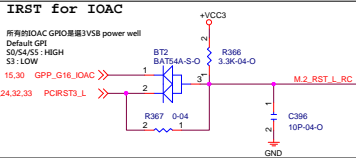
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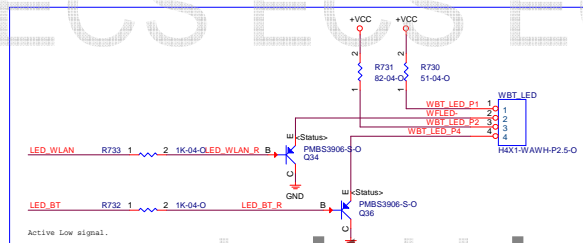
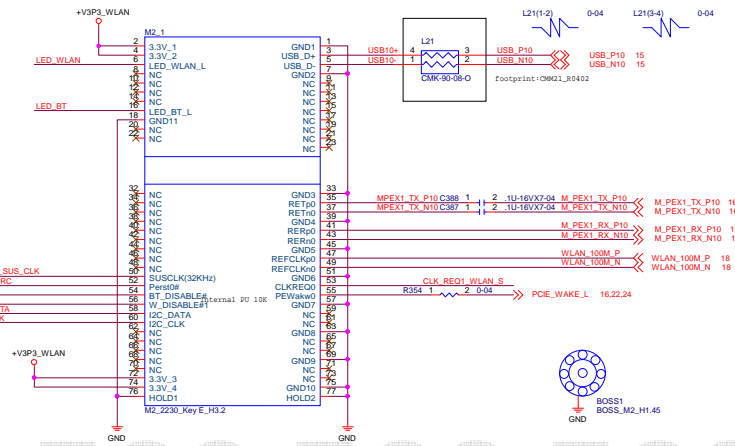
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M.2 (NGFF)

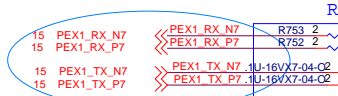
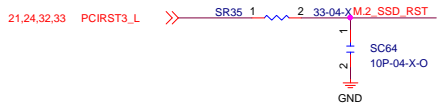


	ATX_PWRGD	+V3P3_WLAN
S0	1	+VCC3
S3/S4/S5	0	+3V5B



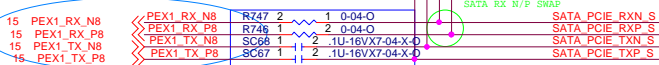
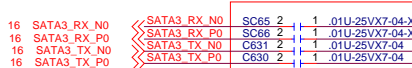
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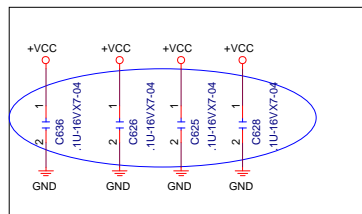


20150312
PCIe Port 7 - 8 Swap for PCI Express Controller Lane Reversal

SATA PCIe Co-lay

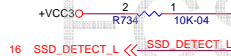


20150312
PCIe Port 7 - 8 Swap for PCI Express Controller Lane Reversal



Stitch CAP

20150119
C636, C626, C625, C628 unstuff -> .1U-16VX7-04
for SI solution.



16 SSD_DETECT_L

SATA RX N/P SWAP

SATA PCIe RXN S

SATA PCIe RXP S

SATA PCIe TXN S

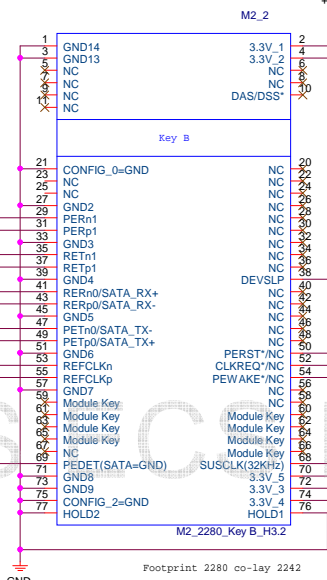
SATA PCIe TXP S

Truth Table

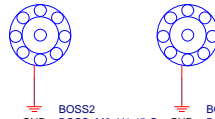
	R1	R2
SATA	V	
PCIe		V

Function	N_in- to N_outb-
L	SATA
H	PCIe

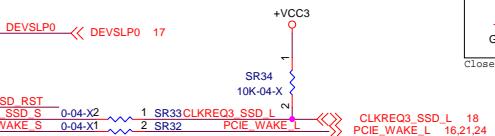
10-456-067068
SLOT.WGP M.2..67P 2P 90D SMD..P.0.5mm
....G/F..KEY B.H3.2..BLACK.APCI0018-P002A....LEAD-FREE(RoHS/HP)..LOTES
(替)10-456-067083



+VCC3



23-745-201155
BOSS..M2*0.4/D5.5*0.65±0.7mm(U&D)..H1.45 d3±4(U&D).
THROUGH.1215...SN...WI-P-G82123A.W/MYALR.....
LEAD-FREE(RoHS/HP)..GREAT GOLD



17 M2 SSD_RST

CLKREQ3 SSD_S 0-04-X2

PCIE_WAKE_S 0-04-X1

CLKREQ3 SSD_L 18

PCIE_WAKE_L 16,21,24

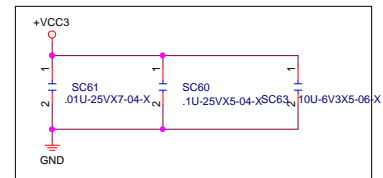
M2 SSD_SUS_CLK

M2 SSD_SUS_CLK 16

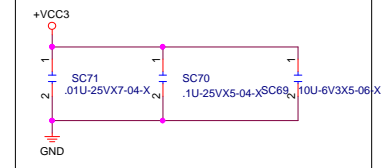
SC62 10P-04-X-O

GND

Footprint 2280 co-lay 2242



Close to Pin 2 4



Close to Pin 70 72 74


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Elitegroup Computer Systems			
Title			
M.2 Slot(SSD)			
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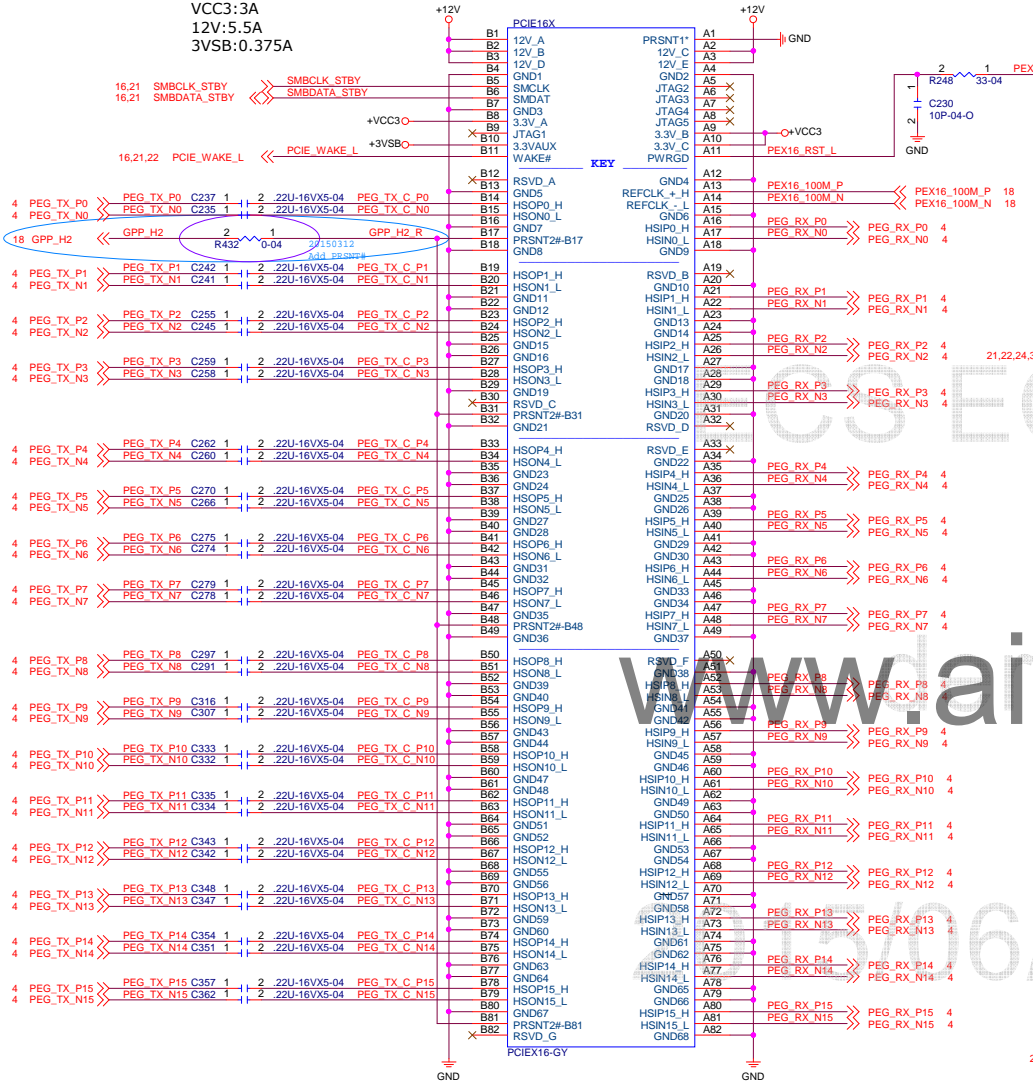
2015/06/02 16:15

		
Title Reserve		
Size Custom	Document Number H11H4-AD2	Rev V1.1
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PCI-E X16 SLOT

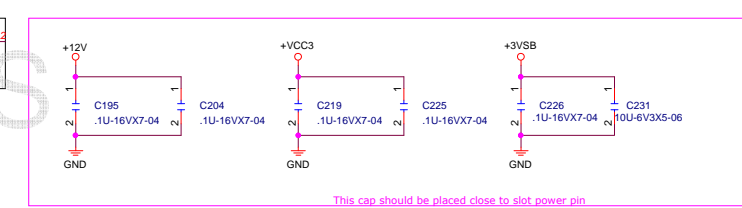
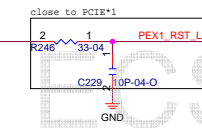
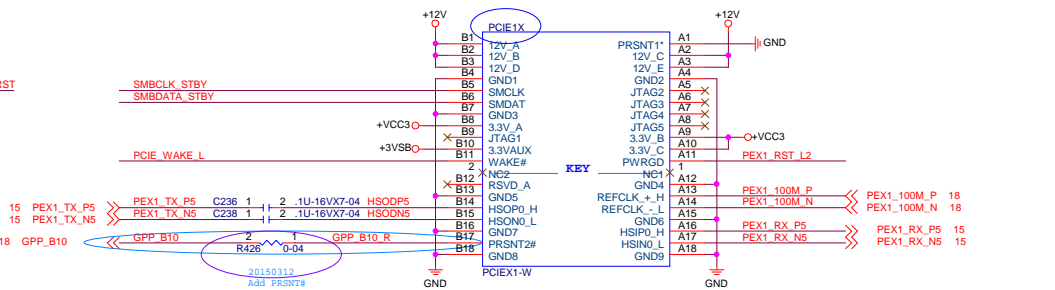
PCI-E SPEC

VCC3:3A
12V:5.5A
3VSB:0.375A

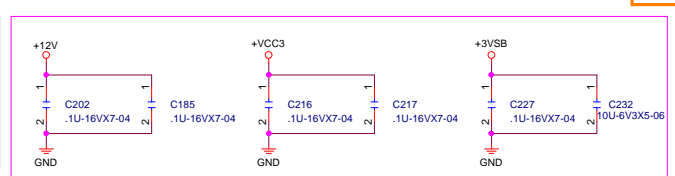
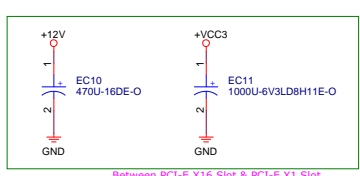
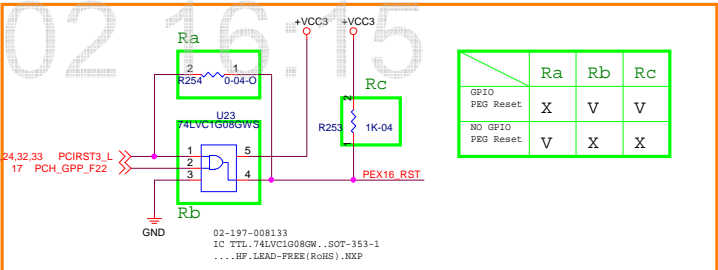


PCI-E X1 SLOT1

20150112
Silk screen PCIE1_1->PCIE1



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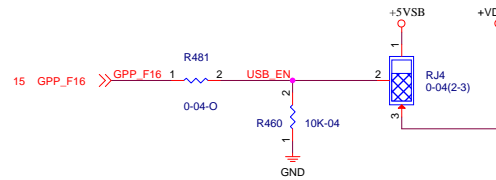
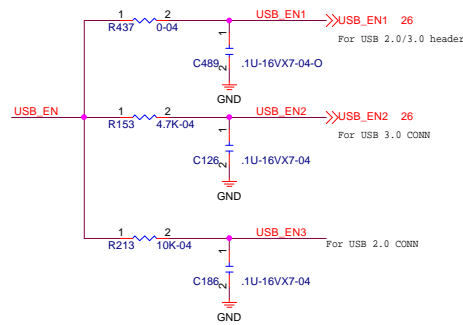


Elitegroup Computer Systems			
Title	PCI-E X16/X1 Slot		
Size	Document Number	H11H4-AD2	Rev
Custom			V1.1
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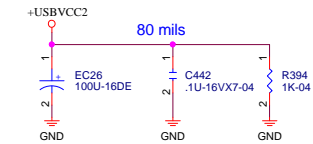
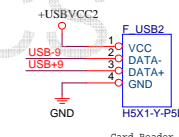
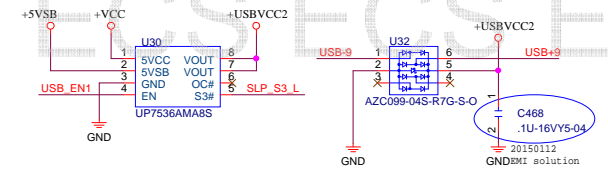
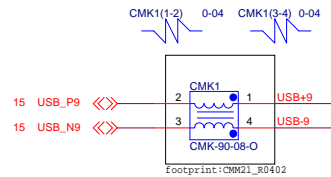
ECS ECS ECS

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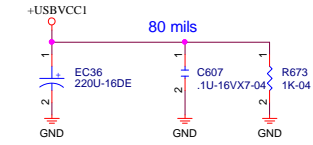
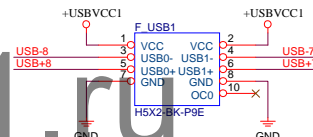
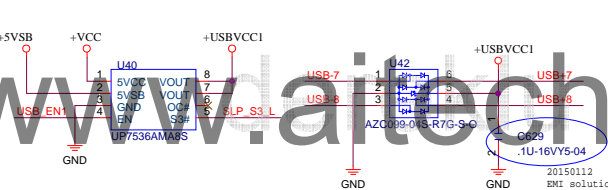
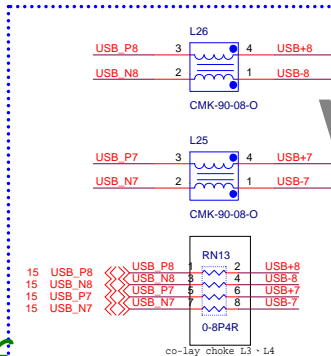
2015/06/02 16:15



uP7536 Enable use	RJ?	RJ?	S4/S5 USB_5V_DUAL	Customer
★ VDIMM	0ohm (1-2)	NA	0 Volt	Acer S4 w/o S5 w/ USB_5VDUAL
5VSB	0ohm (2-3)	NA	5 Volt	
GPIO	NA	0 ohm	S4 : 0 Volt S5 : 5 Volt	



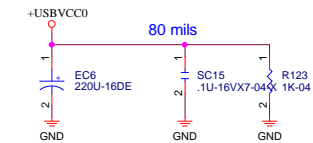
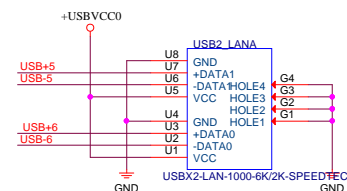
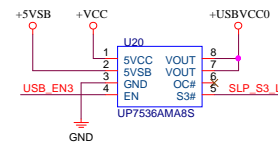
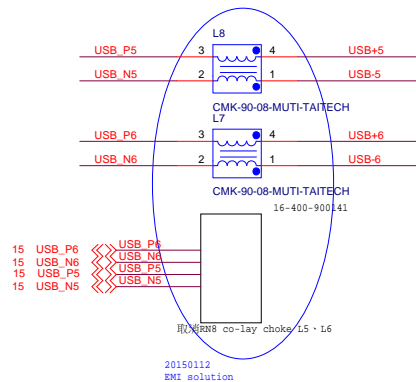
6,15,16,26,32,42,44 SLP_S3_L SLP_S3_L



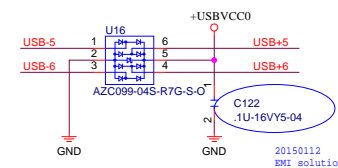
USB2.0 header

USB2.0 connector

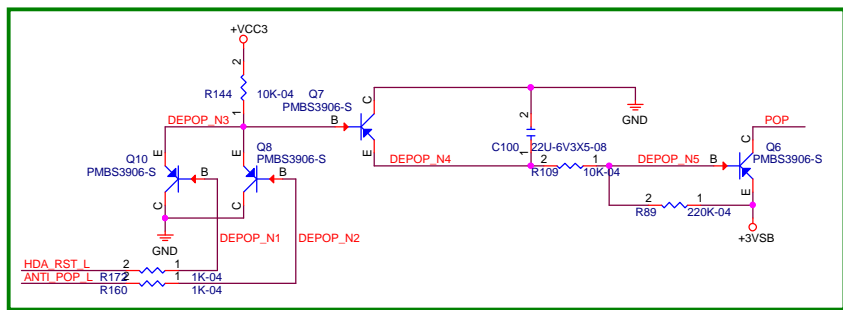
USB2.0 header reserve



Lan + USB2.0

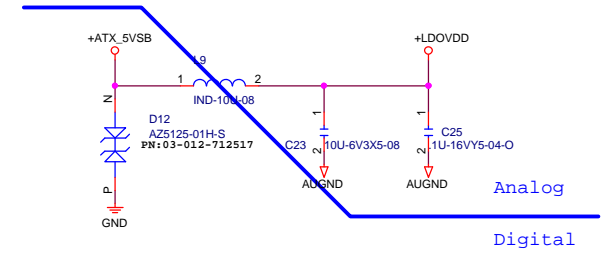
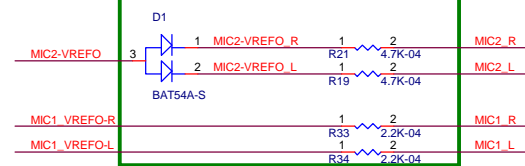


Elitegroup Computer Systems			
Title: USB2.0 Connector/Header			
Size: Custom	Document Number: H11H4-AD2	Rev: V1.1	
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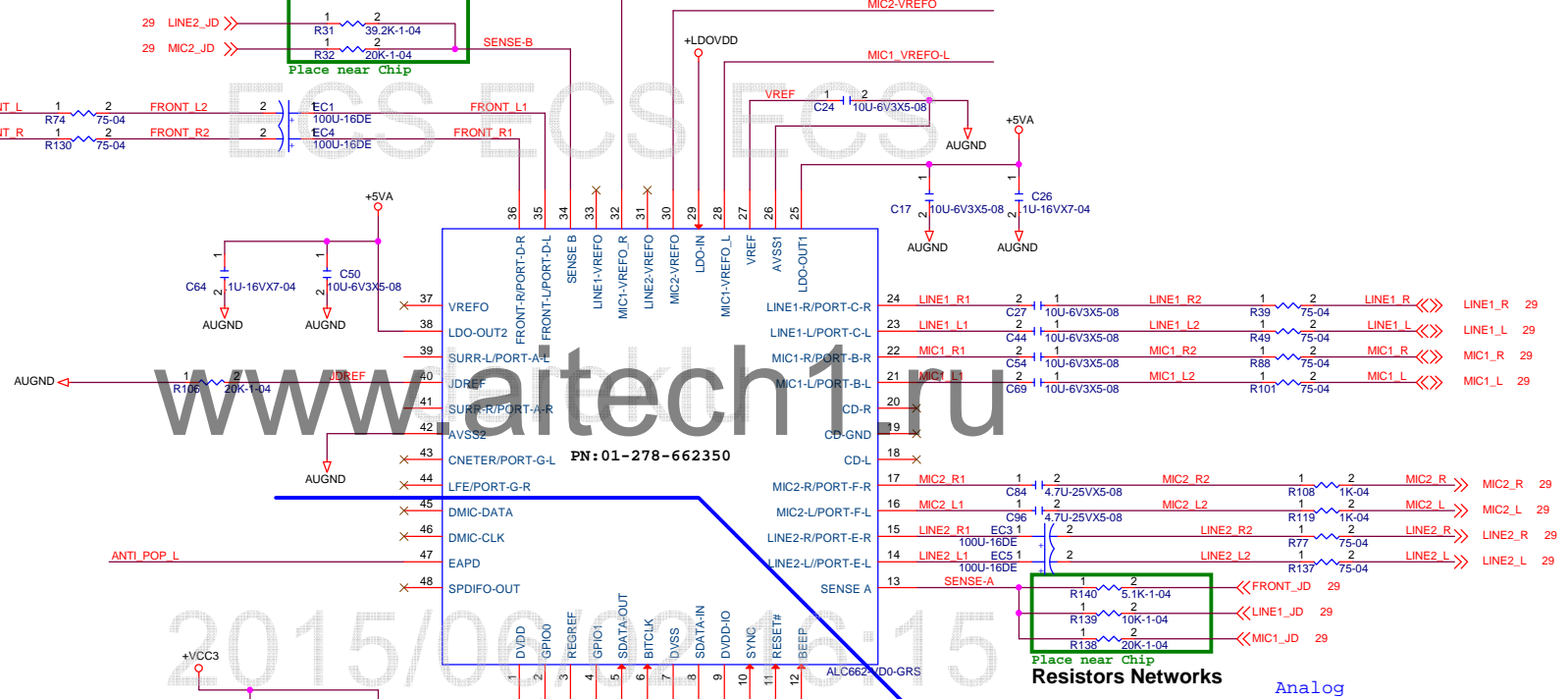


De-pop circuit

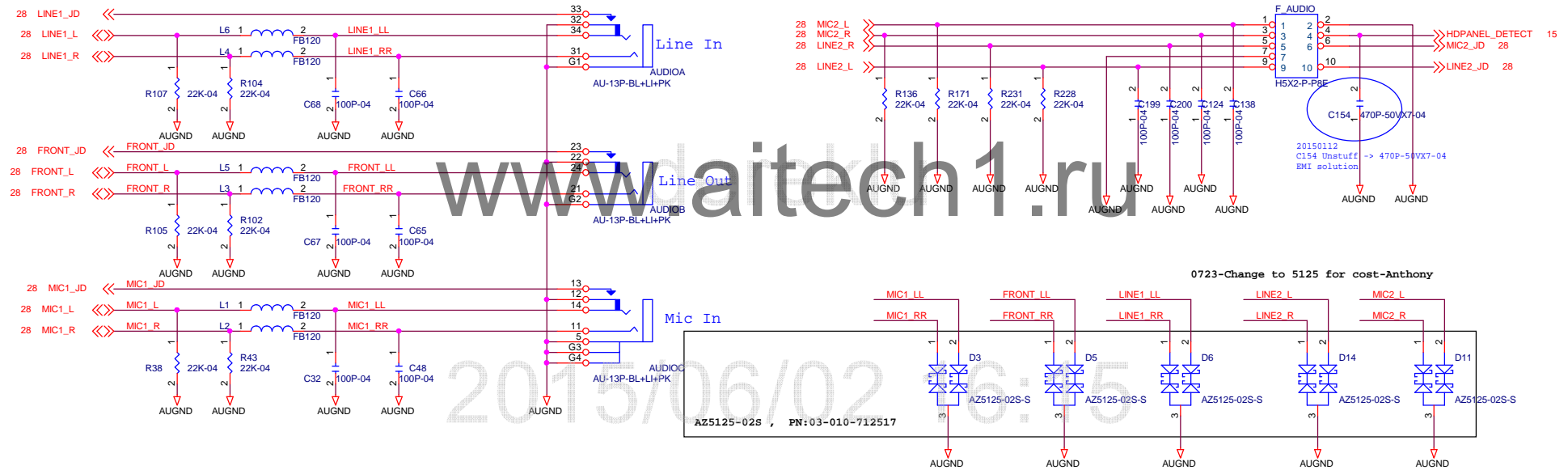
MIC Bias



Resistors Networks

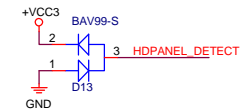


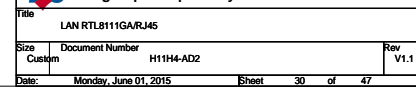
ECS ECS ECS



0815-Acer confirm remove JD TVS

BAV99-S , PN:03-030-709941




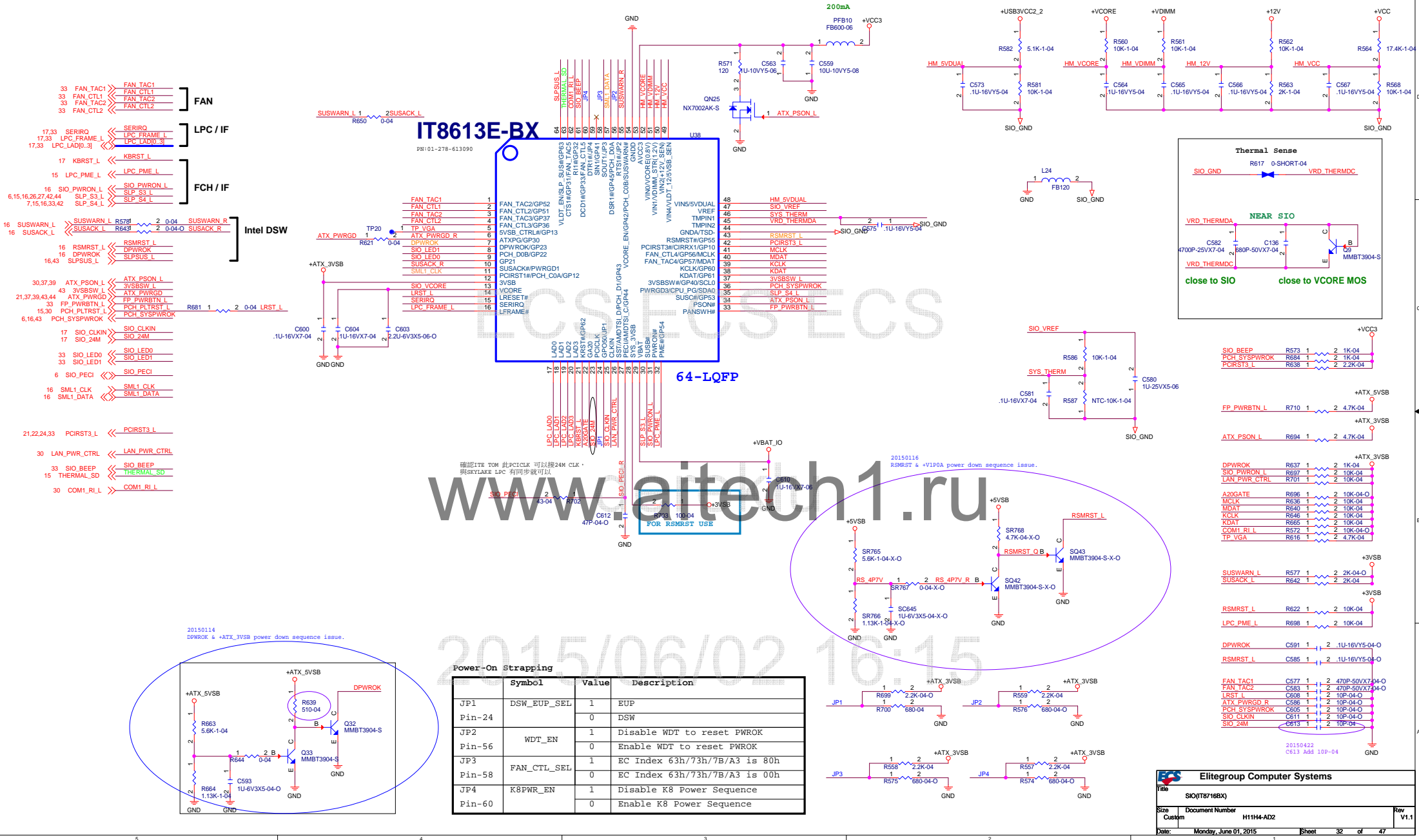


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Power-On Strapping

	Symbol	Value	Description
JP1	DSW_EUP_SEL	1	EUP
Pin-24		0	DSW
JP2	WDT_EN	1	Disable WDT to reset PWROK
Pin-56		0	Enable WDT to reset PWROK
JP3	FAN_CTL_SEL	1	EC Index 63h/73h/7B/A3 is 80h
Pin-58		0	EC Index 63h/73h/7B/A3 is 00h
JP4	K8PWR_EN	1	Disable K8 Power Sequence
Pin-60		0	Enable K8 Power Sequence

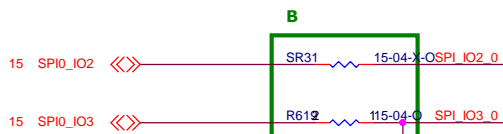
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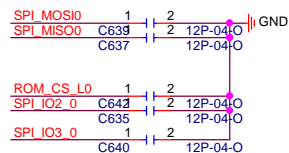
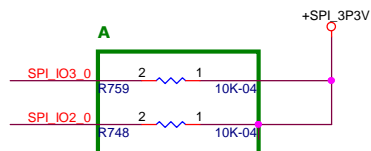
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Title Reserve			
Size	Document Number		Rev
Custom	H11H4-AD2		V1.1
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SPI ROM



R758 2 11K-04-O GND

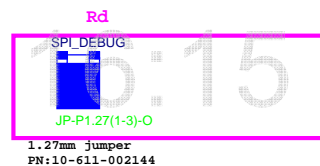
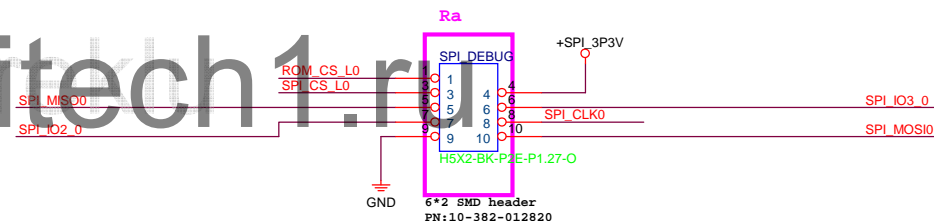
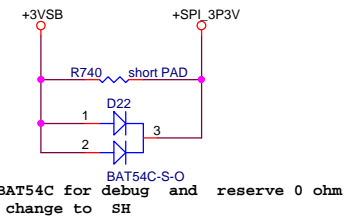
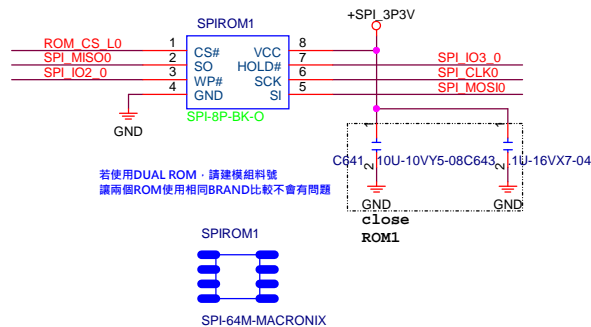
SKL Platforms - SPI0_IO3 Signal Implementation Requirement for ES or pre-ES1/ES1 Samples




SPI mode selection:

MODE \ BIOS WP	A	B
Standard/Dual	NA	10K
Quad	NA	1K

Note. Quad SPI not support WP




	Ra	Rd	Rf
A3~A5	O	O	X
MP	X	X	C

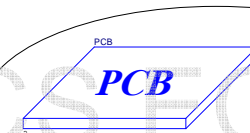
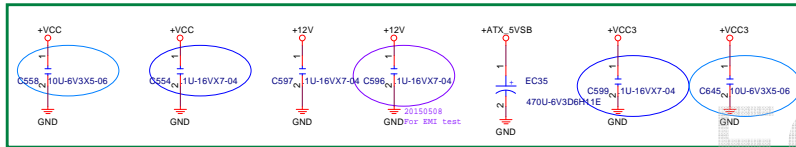
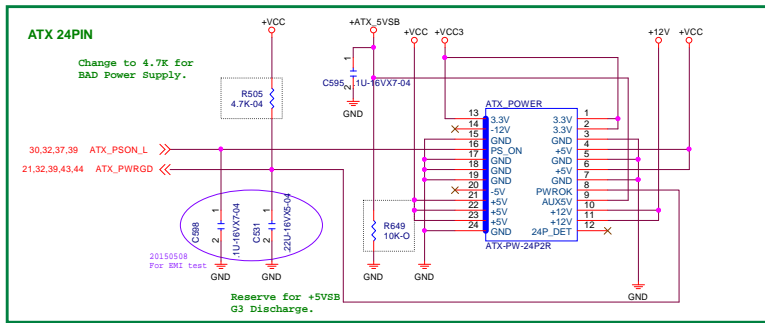
				
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SPI ROM				
Size	Document Number			Rev
B	H11H4-AD2			V1.
Date:	Monday, June 01, 2015	Sheet	35	of 47

ECS ECS ECS

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2015/06/02 16:15

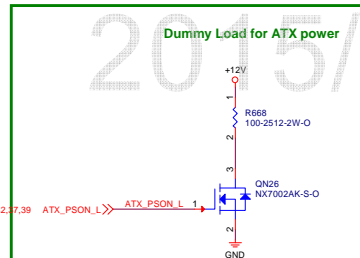
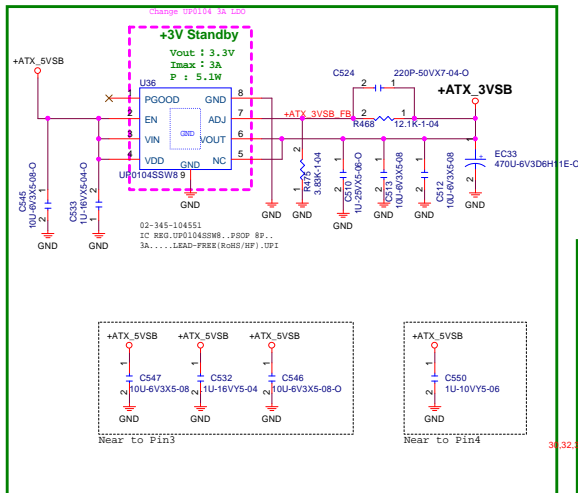
		
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Reserv		
Size	Document Number	
B	H11H4-AD2	
Date:	Monday, June 01, 2015	Sheet 36 of 47
		Rev V1.1



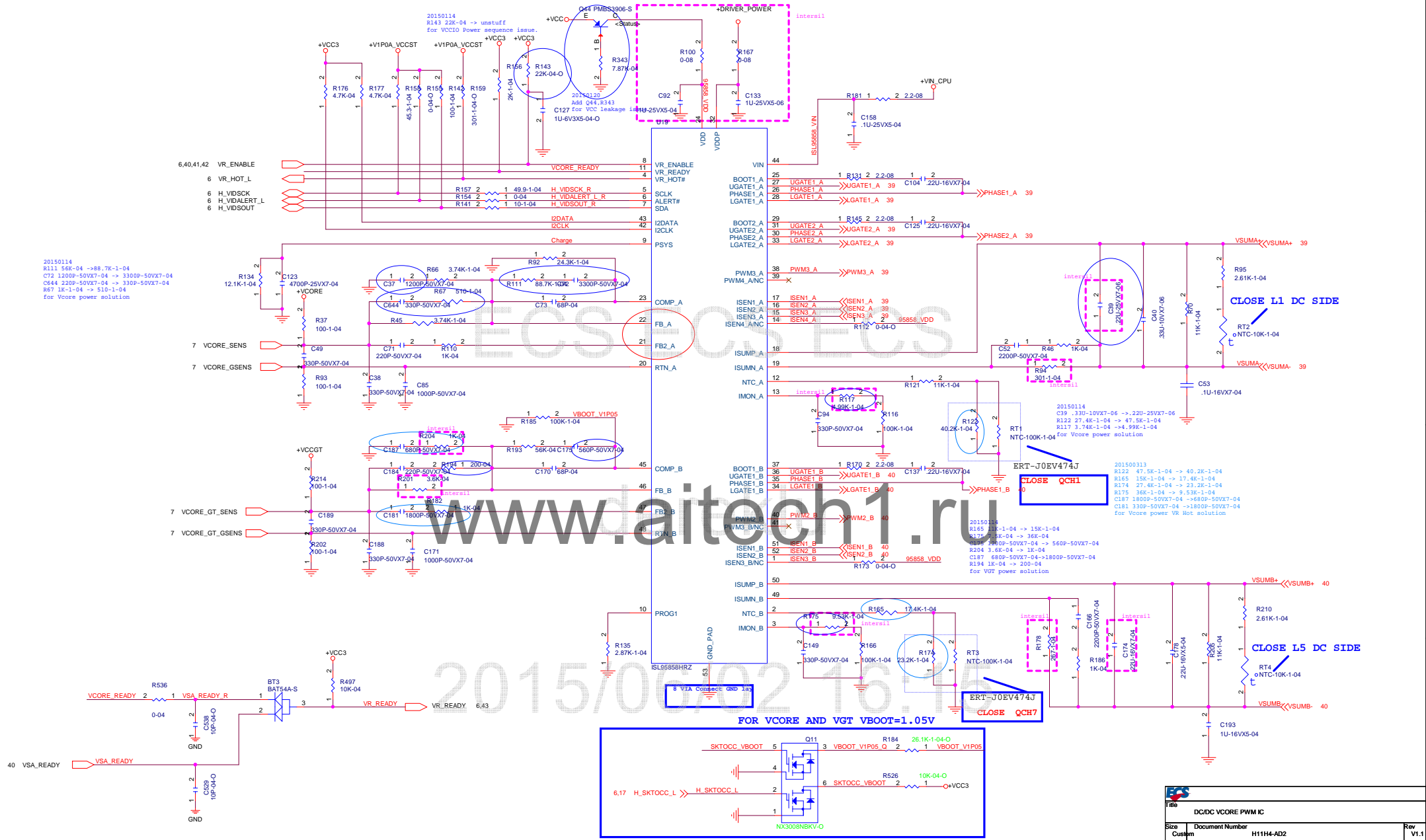
PCB M/S: H1124-AD2... V.B... 244*200*1.6mm, 4L... LEAD-PFREE, GREEN, OSP... GEL


BOM

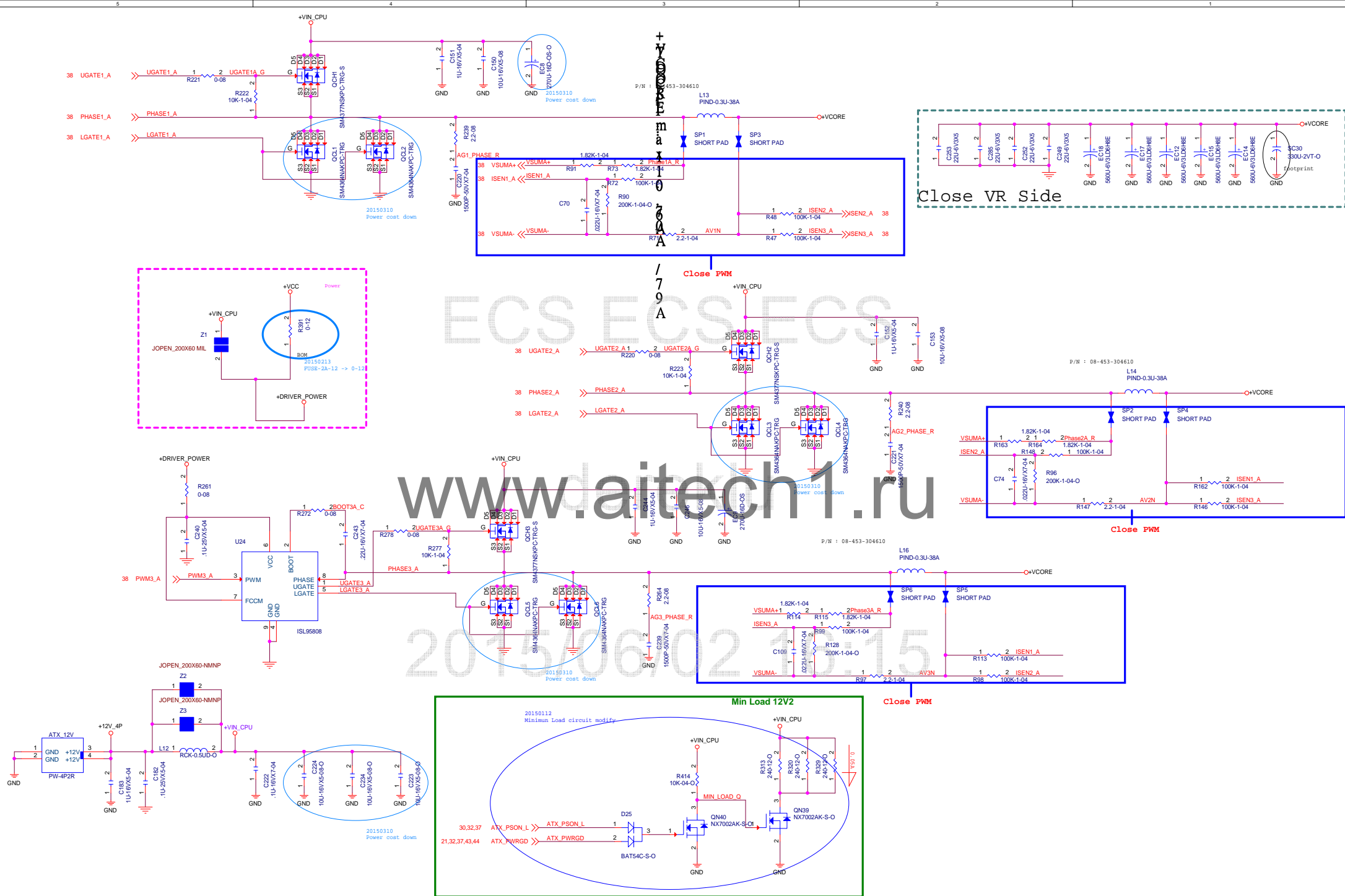
Derek Lu 9/12 Del VCC3 & VCC DC/DC switching



Elitegroup Computer Systems			
File	ATX_24P		
Size	Document Number	H11H4-AD2	Rev V1.1
Custom			
Date:	Monday, June 01, 2015	Sheet 37 of 47	



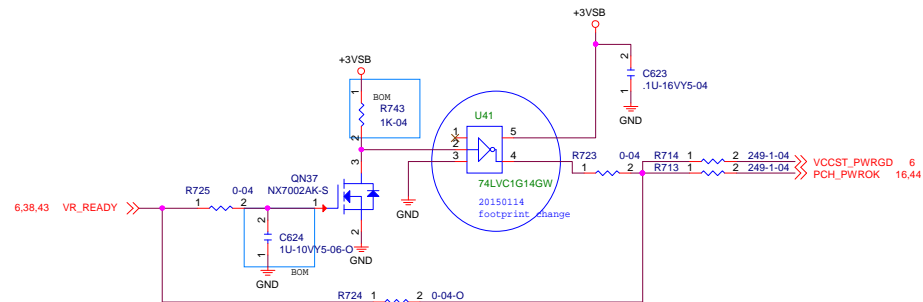
			
Title			
DC/DC VCORE PWM IC			
Size	Document Number		Rev
Custom	H11H4-AD2		V1.1
Date:	Monday, June 01, 2015	Sheet	38 of 47



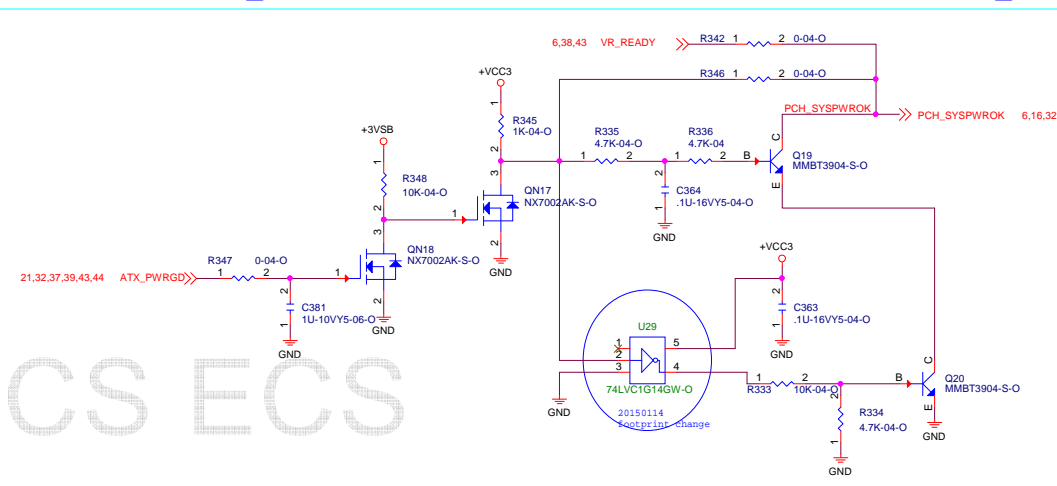
Reserve Dummy Load 12V2 for Consumer EE Design Request Item 2-20

Title			DC/DC Vcore DRIVER IC
Size	Document Number	H11H4-AD2	Rev V1.1
Date:	Monday, June 01, 2015	Sheet	39 of 47

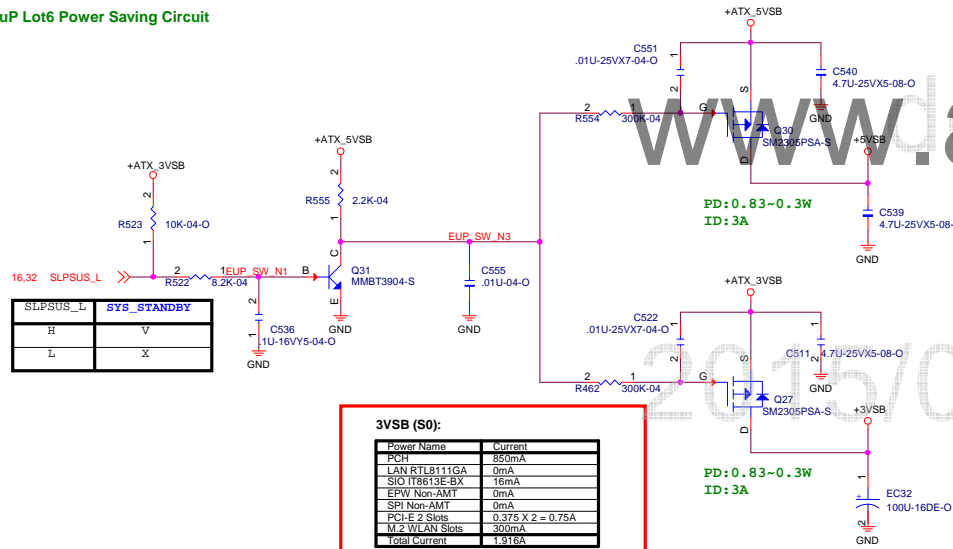
PCH & VCCST PWROK



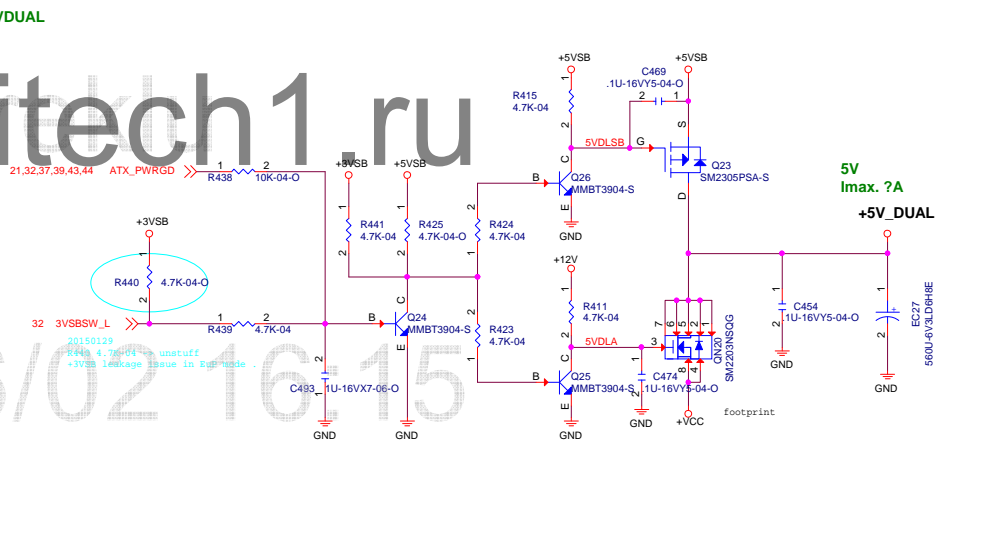
SYS_PWROK SURPRISE POWER DOWN TRIGGERED BY PWRGD_PS




EuP Lot6 Power Saving Circuit

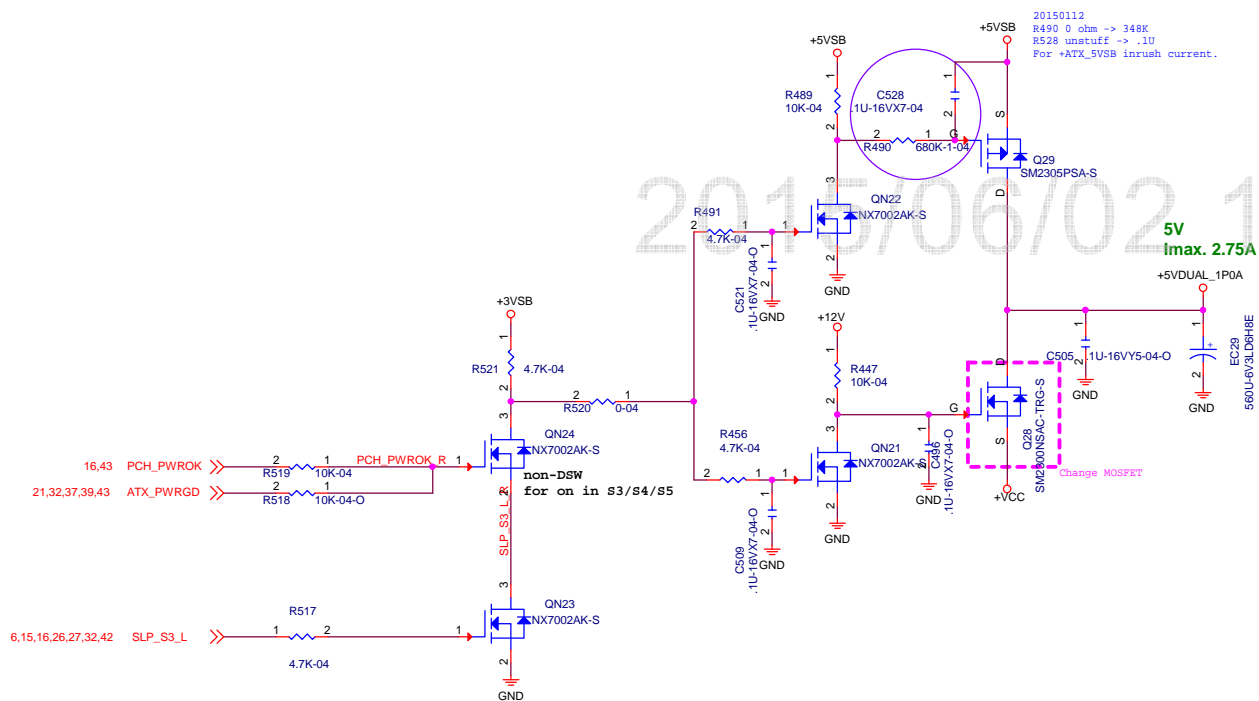
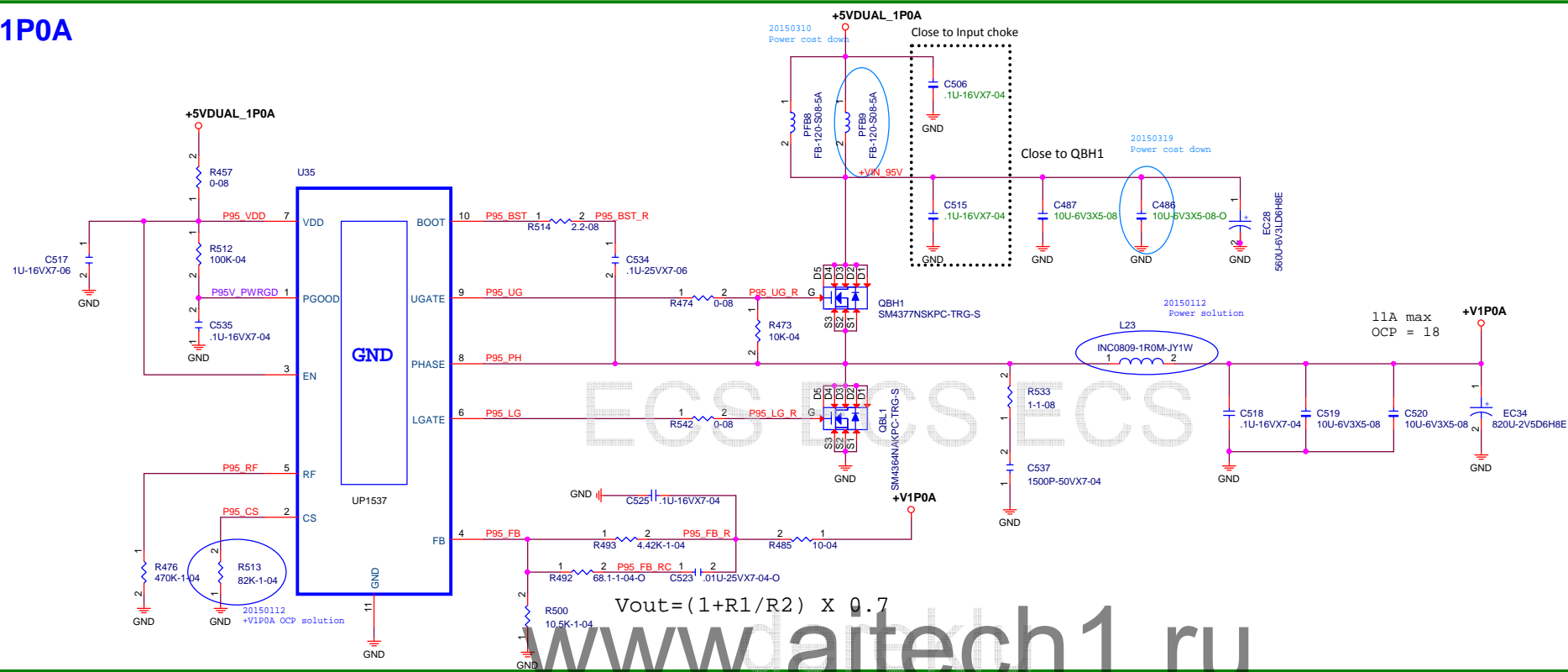


5VDUAL



				
Title DC/DC DDRVPP & 5VDUAL				
Size Custom	Document Number H11H4-AD2			Rev V1
Date: Monday, June 01, 2015	Sheet 43	of 47		

V1P0A



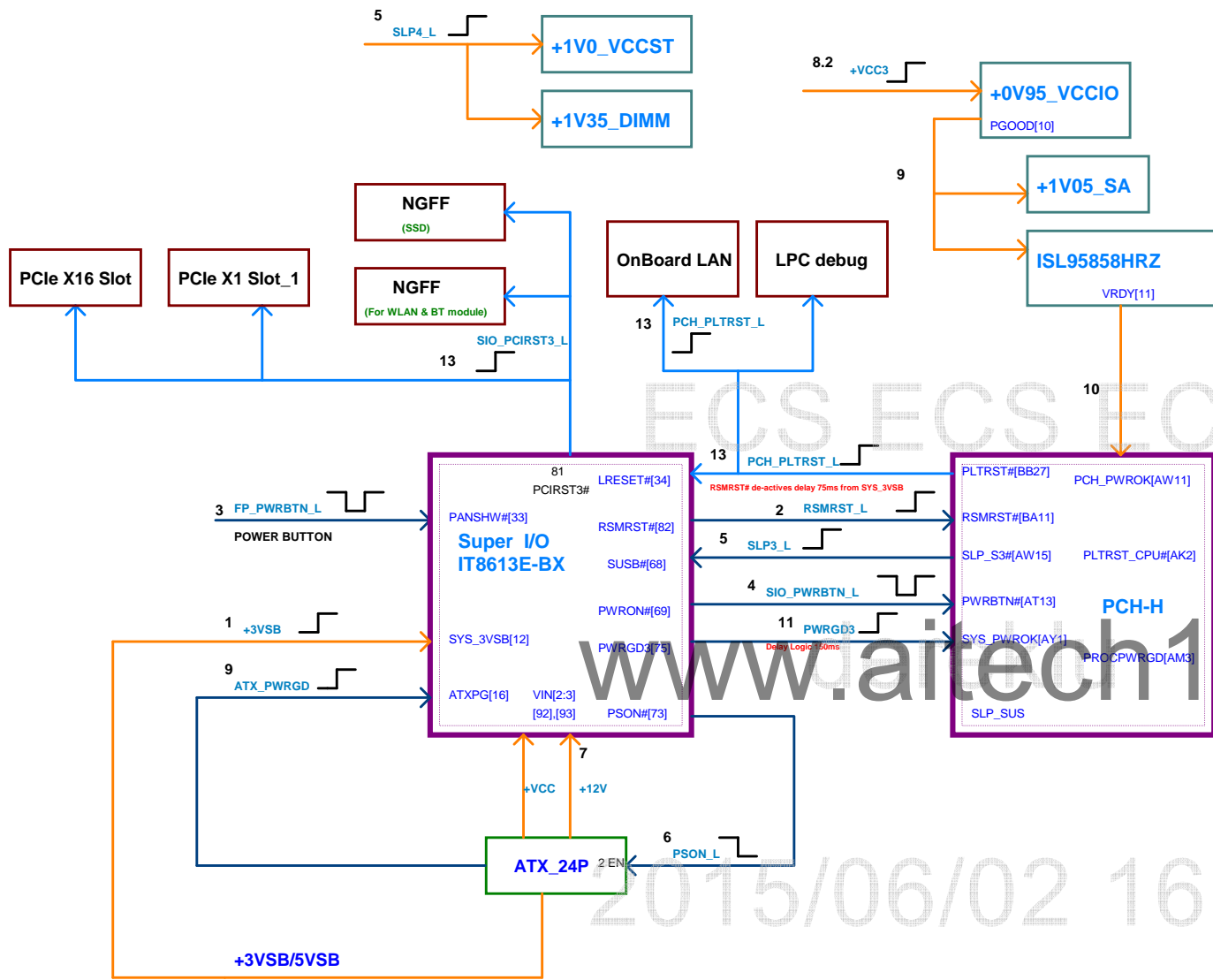


Figure 41-1. SKL S Flow Diagram for SYS_PWROK/PCH_PWROK Generation

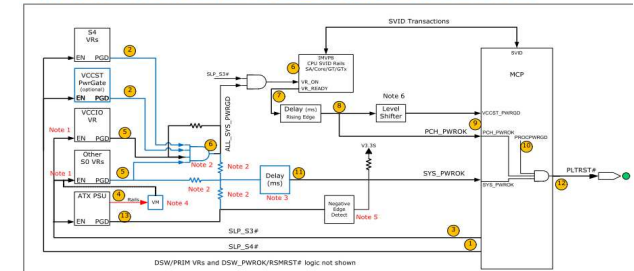


Figure 41-2. SKL S Flow Diagram for RSMRST_PWRGD# Generation

